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Deep p-ring trench termination: An innovative and cost-effective way to reduce silicon area

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Abstract— A new type of high voltage termination, namely the "deep p-ring trench" termination design for high voltage, high power devices is presented and extensively simulated. Termination of such devices consumes a large proportion of the chip size; the proposed design concept not only reduces the termination silicon area required, it also removes the need for an additional mask as is the case of the traditional p+ ring type termination. Furthermore, the presence of the p-ring under and around the bottom of the trench structure reduces the electric field peaks at the corners of the oxide which results in reduced hot carrier injection and improved device reliability.

***Index Terms*—Power Semiconductor Devices, High Voltage, Termination**

I. Introduction

High voltage semiconductor devices require termination regions in order to obtain low electric field peaks at the edges i.e. electric field peak electric field values below the critical breakdown. They are carefully engineered to uniformly distribute the potential to avoid a negative impact on the device breakdown performance. In order to be effective these termination areas must have a higher voltage carrying capability than the interior devices. In this way the voltage rating is given by the interior device (active area) only. Electrical termination can be achieved either by dielectric materials or/and by reverse-biased pn-junctions. Under Dielectric Isolation, dielectric insulator material is used and electrical termination is achieved by forming oxide filled trenches in the area surrounding the device active area. Junction isolation utilises reverse-biased p/n layers.

A significant reduction of chip size has been achieved through the adoption of trench technology for the active area of power MOSFETs and IGBTs. Trench technology not only enabled compact, small chip footprint but also low Rds_{on}. Further, the SuperJunction or RESURF [1, 2] effect has been proved to improve the tradeoff between breakdown and on-state. The concept of p-ring trench IGBT [3,4] was introduced recently and proved extremely effective in reducing the on-state losses without affecting the switching and breakdown characteristics of the device. In the particular study [4], it was demonstrated that a very high density of floating p-regions in the active portion of the device can squeeze the carrier path in the top portion of n-drift region, potentially increasing on-state resistance; this adverse effect was shown to be over-compensated by higher doping of "n-enh" active region. Of equal importance is that no extra cost arises from the formation of this deep p-ring formation.

This paper demonstrates that this technique can be adopted for termination to significantly reduce the termination area. This new termination design features deep p-rings formed at the bottom of trenches in an identical way with what was used for the formation of the active-area deep p-rings i.e. by implanting boron through the trench openings. It is demonstrated through extensive simulations that for a 1.2kV rated device, the termination area is reduced by 30% when compared to a conventional p-ring design.

II. Structure Description

Fig. 1 (a) shows the schematic representation of a conventional p+-ring termination design (termination and active area). For deep (up to 10um) and relatively highly doped regions, this termination design requires an additional mask and therefore extra fabrication cost. A good termination design in such a case translates into evenly distributed electrostatic potential across the device surface. For a 1.2kV rated structure the total lateral width around the device can be up to 450μm. Fig 1(b) shows a full trench isolation using a deep trench filled with dielectric, which dramatically decreases the junction-termination area with a total lateral termination radius of up to about 100μm [5]. The termination breakdown voltage is dependent on the dielectric type and can potentially suffer from Hot Carrier Injection effects due to the exposure of a large area of oxide on high electric fields. Fig.1 (c) shows the proposed new termination design (termination and active area). The formation of p-rings at the bottom of the gate trenches is done through trench etching and direct implantation of boron through the opening before the oxide and polysilicon deposition. This fabrication methodology has been demonstrated and tested for the active area of a Trench IGBT structure. A SEM image of the experimentally demonstrated formation of p-rings under trenches in the active area is shown in Fig. 2.

As shown in the schematic representation of Fig. 1(c), the surface area of this new type of termination utilizes the active area p-body layer. In the active area there exists an n-enhancement layer which has elevated doping concentration. The p- rings therefore serve as charge compensating layers which counterbalance this higher doped n-enhancement layer. In the absence of n-enhancement layer in the termination

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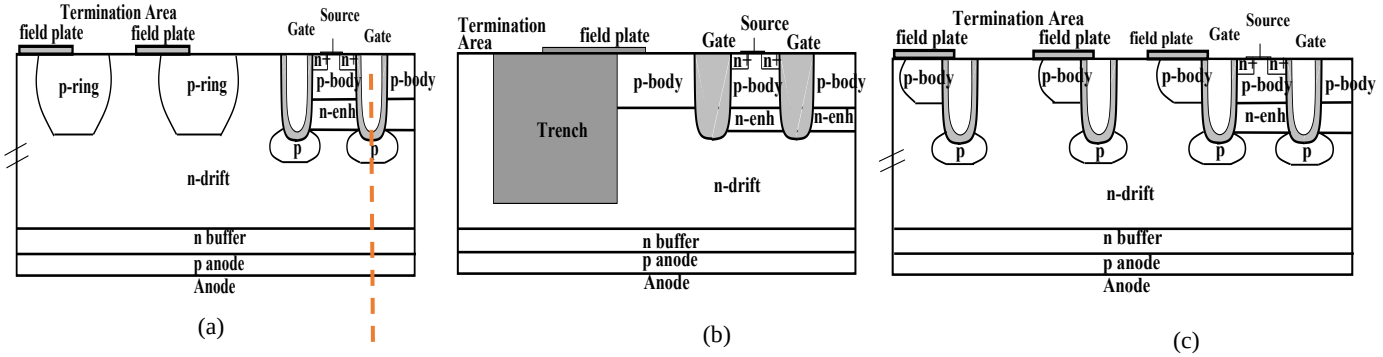

Fig. 1 Schematic representation of the termination structures modelled and simulated. (a) The conventional p+ ring termination structure with the termination region (p+-rings) extending left (not to scale). (b) Schematic cross-section of the Deep Dielectric Termination. (c) The proposed deep p-ring trench termination structure with the termination region (p-rings/p-body rings) extending left.

region, the vertical diffusion of this layer is deeper than the active area. This combination of p-body surface ring with a deep p-ring at the bottom of the trench forms a two-step p-ring layer in the termination area. It should be noted that the p-body appears at the edge of the trenches away from the active area. The edges of this two-step p-ring formation away from the active area are also protected using field plates, lowering the electric field strength and ensuring the electrostatic potential distribution is even throughout the termination. Hence, when compared to the conventional termination where the p+ rings are formed using a separate mask, for the proposed deep p-ring trench termination, the implanted p+ trench rings can reach a comparable depth (around 10um) into silicon. It should be also mentioned that the presence of the deep p-ring under the trench oxide layers not only assists the potential distribution but also protects the oxide from high electric fields and therefore hot carrier injection.

Fig.3 shows a schematic representation of the active and corresponding termination area of a 1.2kV semiconductor device with rings of trenches and p-body tracks surrounding the devices. This new termination can also be applied to planar DMOS type structures in the active area (provided that the extra mask layers are worth the area reduction of the new termination design).

III. Device Simulations and Performance

Extensive process simulations were performed to define the process steps required for the active and termination area to be compatible using Synopsys Sentaurus TCAD. For that, the total p-ring dose, implantation energy and diffusion (i.e. ring dimensions) were optimized. Fig. 2. shows how the p-rings under the trenches are expected to form, also at the termination area. Thereafter a significant number of device simulations were performed to optimize the termination layout. That

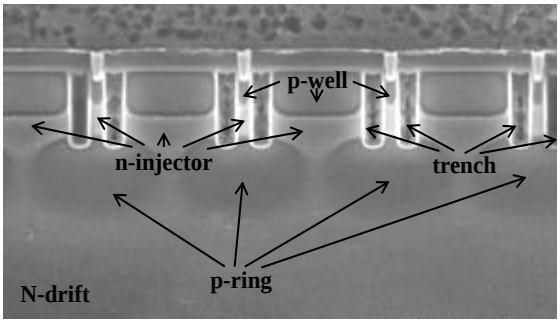

Fig. 2 SEM of the active area showing the p-rings under the trench. The same fabrication process technique is adopted for termination [3]

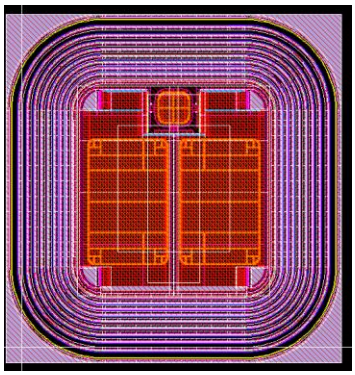

Fig. 3. A layout representation of the active (grey area) and corresponding termination area of a 1.2kV semiconductor device with rings tracks surrounding the devices.

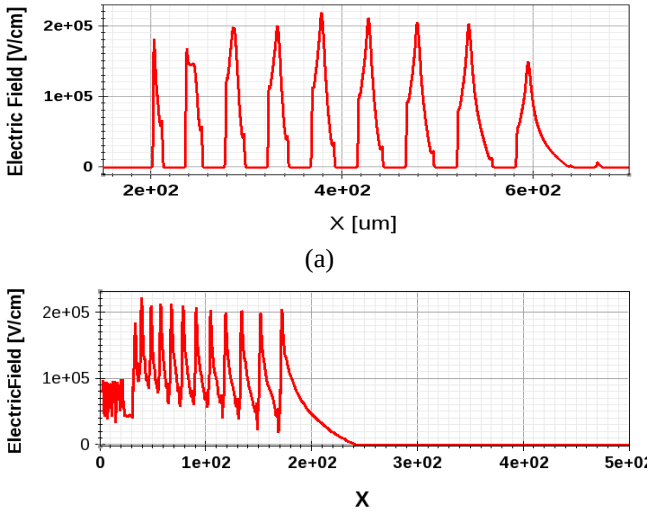

Fig. 4. The electric field distribution of (a) the conventional p-rings and (b) the deep trench p-ring termination.

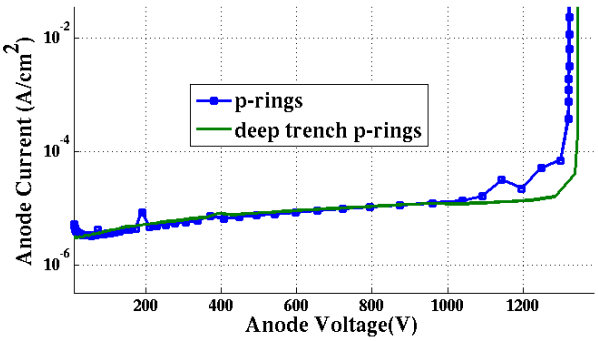

Figure 5. The simulated breakdown voltage of the deep trench p-ring and p-rings (conventional) type termination designs.

includes the optimization of the required distance between them, to achieve the desired voltage with the minimum possible silicon area. To assess the performance of the proposed termination, extensive simulations were performed to also optimize the termination structures of Fig. 1 (a) and Fig. 1 (b). The devices were simulated with an assumed rotational symmetric geometry which accounts for the field enhancement at the periphery due to the resulting spherical junctions [6-9].

The proposed deep p-ring trench termination achieved the breakdown of more than 1.2kV within less than 200µm of silicon area. For this, 11 trenches with p-rings were used for which the spacing between them increasing as we move away from the active area. Fig. 4 shows the electric field distribution at breakdown along a horizontal line through the peak E-Fields. The electric field peaks between each pair of rings (more precisely at the physical edge of each p-ring, at the junction between the p-ring and the n surface) are balanced, which means that the termination has optimized spacing length. The resulting layout design is shown in Fig. 3. The blocking IV curve is shown in Fig. 5.

Fig.6 shows the electrostatic potential distribution at 1.2kV for the proposed structure and it is compared with the conventional

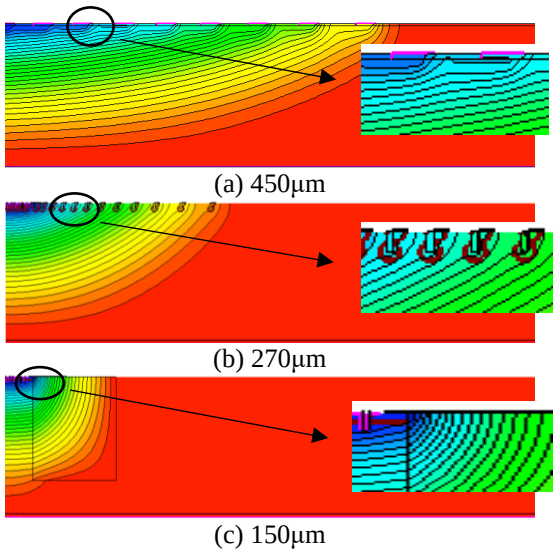

Fig. 6. The electrostatic potential distribution for optimised termination structures at breakdown. (a) Conventional p+ rings, (b) deep p-ring trench (c) Deep Dielectric termination.

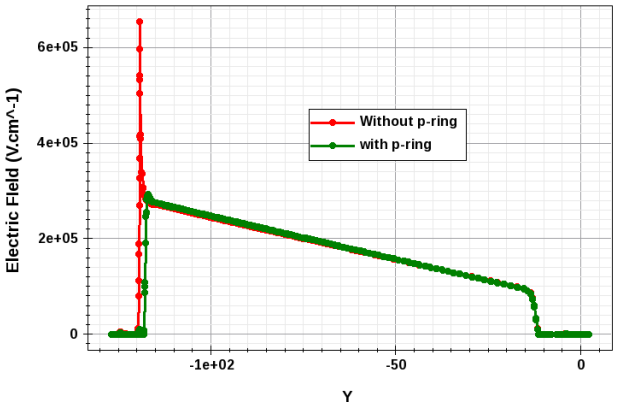

Figure 7. The electric field distribution across a cutline running through the active area gate trench with and without the presence of the under-the-gate p-ring (vertical cutline as shown in figure 1(a)).

p+ ring termination and the Deep Dielectric termination. From this figure, we can see that the electrostatic potential drops to zero within the termination regions. As shown the Deep Dielectric termination is still the most compact design, with the required termination length being about 150µm. The conventional (optimised) floating rings termination design requires about 450µm. The novel termination design proposed in this paper can support the required voltage with 270µm of termination length. That corresponds to more than 30% reduction in the required area. At the same time, it is more cost effective than both other options, because there is no need for an extra mask to form the p+ ring termination. Since the proposed design has the p-rings under the trenches, no issues with hot carrier injection are expected. Indeed, Fig.7 shows the electric field distribution across a cutline running through the active area gate trench with and without the presence of the under-the-gate p-ring [3,4]. Furthermore, when compared to the Deep Dielectric termination, which is the most compact, no deep trenches are needed, and no need for new and unproven materials are needed.

IV. Conclusion

In this letter, we propose new termination design which reduces the required termination length by 30%. The advantage of the proposed structured is also due to the reduced cost and fabrication complexity as well as due to the expected highly reliable performance. When compared to other innovative solutions, e.g. the Deep Dielectric termination, the fabrication does not need very deep trenches nor additional steps, masks or new dielectrics. Also because the oxide is protected by the p-rings, it does not have to withstand high electric fields and therefore, it is not likely to suffer from hot carrier injection. Therefore, the proposed structure not only is a very compact structure, it achieves that without the requirement of extra cost, it introduces no additional technical nor fabrication difficulties. Indeed, we believe that this structure is the most promising and fabrication-friendly termination design for trench MOSFETs and IGBTs.

REFERENCES

[1] L. Lorenz, G. Deboy, A. Knapp, and M. Marz, “COOLMOS—A new milestone in high voltage power MOS,” in Proc. 11th Int. Symp. Power Semiconductor Device ICs, 1999, pp. 3–10.

[2] J. A. Appels and H. M. J. Vaes, "High voltage thin layer devices (RESURF devices)," 1979 International Electron Devices Meeting, Washington, DC, USA, 1979, pp. 238-241.

[3] M Antoniou, N Lophitis, F Udrea, F Bauer, I Nistor, M Bellini, M Rahimo, “Experimental demonstration of the p-ring FS+ Trench IGBT concept: A new design for minimizing the conduction losses,” *in Proc. IEEE International Symposium on Power Semiconductor Devices & IC's (ISPSD), 2015, pp. 21-24.*

[4] M. Antoniou, N. Lophitis, F. Bauer, I. Nistor, M. Bellini, M. Rahimo, G. Amaratunga, F. Udrea, "Novel Approach Toward Plasma Enhancement in Trench-Insulated Gate Bipolar Transistors," in IEEE Electron Device Letters, vol. 36, no. 8, pp. 823-825, Aug. 2015.

[5] Théolier L, Mahfoz-Kotb H, Isoird K, Morancho F, Assié-Souleille S, Mauran N. A new junction termination using a deep trench filled with BenzoCycloButene. IEEE Electron Device Letters. 2009 Jun. 30(6):687-9.

[6] Y. C. Kao and E. D. Wolley, “High-voltage planar p-n junctions,” *Proc. IEEE*, vol. 55, no. 8, pp. 1409–1414, Aug. 1967.

[7] K. P. Brieger, W. Gerlach, and J. Pelka, “Blocking capability of planar devices with field limiting rings,” *Solid State Electron.*, vol. 26, no. 8, pp. 739–745, Aug. 1983.

[8] C. Mingues and G. Charitat, “Efficiency of junction termination techniquesvs. oxide trapped charges,” in *Proc. IEEE Int. Symp. Power Semicond.Devices ICs*, 1997, pp. 137–140.

[9] G. Deboy, J. Tihanyi, H. Strack, H. Gassel, J. Stengl, and H. Weber, “High voltage resistance edge structure for semiconductor components,” U.S.Patent 6 870 201 B1, Mar. 22, 2005.