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EMI Mitigation for SiC Power Module with Chip-on-Ceramic Heatsink Packaging

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***Abstract*—This letter proposes the use of a chip-on-ceramic heatsink packaging to reduce common-mode (CM) noise at the package level while improving thermal performance for SiC power modules. The packaging directly attaches the SiC MOSFETs to a metallized AlN ceramic heatsink, reducing CM capacitive coupling between the switching node and ground, thereby decreasing CM noise. A 400 V to 200 V DC-DC buck converter is built to validate the effectiveness of the packaging in mitigating CM noise. The experimental results demonstrate a reduction in CM current, with a decrease of over 5 dB between 5 MHz and 20 MHz frequency spectrum for the chip-on-ceramic heatsink power module compared to a conventional non-baseplate module. Thermal test results indicate that the ceramic module exhibits better thermal performance than the conventional module, due to the reduced layers between the heatsink and the dice.**

***Index Terms*—Common-mode (CM) noise, chip-on-ceramic heatsink packaging, high dv/dt, power module, SiC MOSFET.**

I. Introduction

COMPARED with Si-based devices, wide bandgap (WBG) devices, such as silicon carbide (SiC) MOSFETs, are increasingly utilized due to their superior characteristics such as fast switching speed and low switching losses. However, the rapid switching characteristics of WBG devices generate high dv/dt at the output node of the power converter, which induces displacement currents via the parasitic capacitance between the switching node and the protective earth (PE), resulting in common-mode (CM) noise [1], [2]. This CM noise is transmitted into the grid through the input power cable of power converters, potentially disrupting the functionality of adjacent electrical equipment and thus hindering the full exploitation of WBG devices' capabilities in various applications.

To mitigate the CM noise, electromagnetic interference (EMI) filters are commonly used [3]. However, these filters are typically large, negatively impacting system power density and efficiency. To decrease the size and weight of EMI filters, it is crucial to reduce the inherent CM noise produced by power converters. Various methods have been proposed to address this issue, including passive cancellation [4], balanced converters [5], the CM voltage cancellation (CMVC) method [3], and integrating package level EMI filters [6], [7], all of which typically require additional components or windings to reduce CM noise effectively. Alternatively, methods like modulation algorithms [8] and balanced topologies [9] can mitigate CM noise without the need for extra components, although their application is constrained to specific topologies. Furthermore, researchers have explored optimizing the power module packaging to reduce CM noise, such as by using materials with low permittivity [10] or employing stacked direct bonded copper (DBC) substrates [11]–[13]. However, these approaches can compromise thermal performance due to the lower conductivity of materials with low permittivity or by increasing the thermal transfer distance with stacked substrates. Thus, while these advanced power module packaging can potentially reduce CM noise, they often entail trade-offs in thermal efficiency that must be carefully considered.

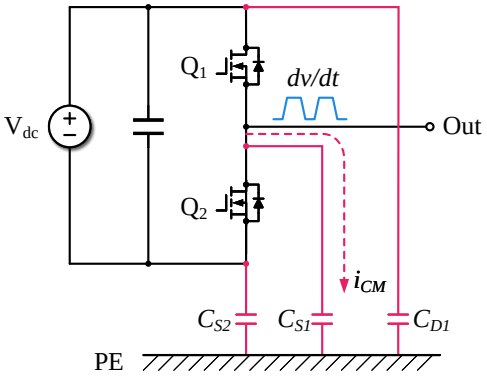

Fig. 1. Circuit of the half-bridge power converter with parasitic parameters.

This letter proposes the use of a chip-on-ceramic heatsink structure to reduce common-mode (CM) noise at the package level while improving thermal performance for SiC power modules. In this module configuration, SiC MOSFETs are directly attached to a metallized ceramic heatsink, which eliminates the need for substrates, aluminum alloy heatsinks and thermal interface material (TIM). The thermal properties of this package structure are investigated in [14]–[17], but no research has been conducted on its EMI properties. In this study, the EMI performance of a chip-on-ceramic heatsink power module is experimentally verified and compared with a conventional non-baseplate module based on our previous work in [16].

The rest of this letter is organized as follows. Section II presents the mechanism of a CM cancellation method at the package level. Section III details the construction of a buck converter using different types of power modules to experimentally validate the CM cancellation approach, with

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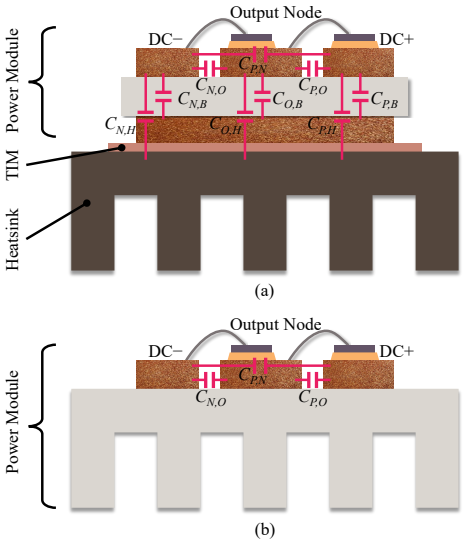


Fig. 2. Schematic illustration for parasitic capacitance of half-bridge power modules. (a) Conventional non-baseplate power module. (b) Chip-on-ceramic heatsink structure for EMI mitigation.

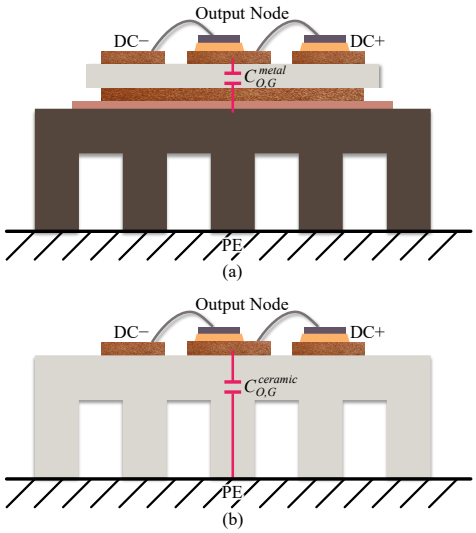


Fig. 3. Modeling of the parasitic capacitance which causes the CM noise. (a) Conventional package. (b) Ceramic package.

an examination of thermal performance also included. Section IV discusses the advantages and disadvantages of the chip-on-ceramic heatsink package. Finally, Section V concludes this letter.

II. Modelling of the EMI

Fig. 1 illustrates the parasitic capacitance within a half-bridge power converter, which arises between each conductive track and the PE. The high dv/dt at the output node of the phase leg introduces a CM current, which can be expressed as

$$i_{CM} = C_{S1}\frac{dv}{dt} \tag{1}$$

From (1), it is evident that reducing the parasitic capacitance C_{Si} between middle conductive track and the PE is an effective method to decrease the CM current.

Fig. 2(a) depicts the parasitic capacitance in a conventional non-baseplate power module that is mounted on a metal heatsink. The parasitic capacitance arises among the conductive tracks ($C_{N,O}$, $C_{P,N}$, $C_{P,O}$), the bottom metal plate ($C_{N,B}$, $C_{O,B}$, $C_{P,B}$), and the heatsink ($C_{N,H}$, $C_{O,H}$, $C_{P,H}$). To reduce the parasitic capacitance, eliminating the bottom copper layer and replacing the aluminum alloy heatsink with and insulated one is an effective approach. Fig. 2(b) shows the parasitic capacitance in a chip-on-ceramic heatsink power module, where the parasitic capacitance is reduced due to the fewer metal components in the module.

During the operation of the power converter, the CM noise primarily originates from the parasitic capacitance between the middle output node and the ground, due to the high dv/dt occuring at this node. Fig. 3 illustrates the modeling of the parasitic capacitance responsible for the CM noise. Specifically, the parasitic capacitance of the power loop can be characterized as the capacitance between the output trace and the PE, and can be expressed as follows

$$C_{O,PE} = \varepsilon_0\varepsilon_r\frac{A_O}{h_{O,PE}} \tag{2}$$

where ε_0 represents the permittivity of free space, and ε_r denotes the relative permittivity of the material filling the space between middle output tracks and the ground. A_O corresponds to the area of the middle output tracks, and $h_{O,PE}$ is the distance between the middle node and the ground.

In conventional power modules, metal heatsinks that are installed or exposed outside the chassis of the power electronics system are typically grounded for safety reasons. The parasitic capacitance of the power loop in such setups can be described by combining the parasitic capacitance between the middle output node and the bottom copper plate with the parasitic capacitance between the bottom copper plate and the heatsink. This configuration outlines how the multiple layers of conductive and insulative materials in the module contribute to the overall parasitic capacitance, impacting the module's EMI performance and susceptibility to CM noise. The parasitic capacitance can be expressed as

$$\frac{1}{C_{O,PE}^{metal}} = \frac{1}{C_{O,B}^{metal}} + \frac{1}{C_{B,G}^{metal}} \tag{3}$$

$$C_{O,PE}^{metal} = \frac{\varepsilon_0\varepsilon_r^{AlN}\varepsilon_r^{TIM}A_OA_B}{\varepsilon_r^{TIM}A_Bh_{AlN} + \varepsilon_r^{AlN}A_Oh_{TIM}} \tag{4}$$

where ε_r^{AlN} is the relative permittivity of the aluminum nitride (AlN) ceramic, which is approximately 8.8, and ε_r^{TIM} is the relative permittivity of the thermal interface material (TIM), typically ranging from 2.2 to 10. In general, the TIM layer is considerably thinner than the ceramic insulation layer. Moreover, the area of the bottom plate, denoted A_B is larger than the area of the middle output track A_O. Therefore, the expression (4) can be simplified as

$$C_{O,PE}^{metal} = \varepsilon_0\varepsilon_r^{AlN}\frac{A_O}{h_{AlN}} \tag{5}$$

which is close to the parasitic capacitance between middle output track and the bottom metal layer.

For ceramic heatsinks, which are insulative materials, there is no requirement for grounding, allowing them to be safely exposed outside. Assuming the chip-on-ceramic heatsink power module is positioned on a grounded metal plate, the total parasitic capacitance can be considered as the sum of the parasitic capacitance in the fin area and the area without fins. When the ceramic heatsink material is AlN, this total parasitic capacitance can be expressed as

$$C_{O,PE}^{ceramic} = \frac{\varepsilon_0 \varepsilon_r^{AlN} A_O^{fin}}{h_{hs}} + \frac{\varepsilon_0 \varepsilon_r^{AlN} A_O^{base}}{\varepsilon_r^{AlN} h_{fin} + h_{base}} \tag{6}$$

Considering that the length of the fins is significantly greater than the thickness of the base of the heatsink and approximately equal to the height of the heatsink, the equation (6) can be simplified as

$$C_{O,PE}^{ceramic} = \varepsilon_0 \varepsilon_r^{AlN} \frac{A_O}{h_{hs}} - \varepsilon_0 (\varepsilon_r^{AlN} - 1) \frac{A_O^{base}}{h_{hs}} \tag{7}$$

Comparing equations (5) and (7), it can be seen that the parasitic capacitance of the chip-on-ceramic heatsink module is smaller than that of the conventional module. This reduction is attributed to the longer distance between the middle output track and the PE in the chip-on-ceramic heatsink configuration.

III. Experimental Verification

A. Test Samples Preparation

To evaluate the EMI performance between different packaging configurations, three types of power modules are manufactured and compared, including a half-bridge chip-on-ceramic heatsink power module, a conventional module with a single substrate (mounted on a 6063 aluminum alloy heatsink), and a conventional one with stacked substrates, as shown in Fig. 4. For the conventional module, compared to the single substrate structure, the module with stacked substrates increases the distance between the switching node and the ground, thereby reducing the $C_{O,PE}$. However, the increased thickness and additional layer of the substrate also lead to degraded thermal performance. 1200 V SiC MOSFETs (CPM2-1200-0080A) are selected as the switching devices for the three modules. The conductive trace layout and heatsink size are same to the previous work in [16].

Fig. 5 illustrates the manufacturing process for the ceramic package. The process begins with the fabrication of the ceramic heatsink, made of AlN, using isostatic pressing technology. After the heatsink is fabricated, active metal brazing (AMB) is applied to attach a copper layer onto the ceramic heatsink. Following this, die attaching, wire bonding, and terminal soldering are carried out. These three procedures align with the traditional methods employed in module manufacturing.

In this work, the prototype is designed and manufactured to verify the concept. To simplify testing, the plastic case installation and encapsulant filling are omitted, as shown in Fig. 4. In practical power electronics applications, the module

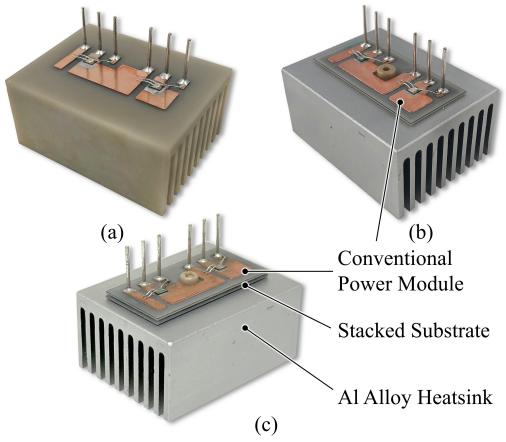


Fig. 4. Power modules for EMI performance characterizing. (a) Chip-on-ceramic heatsink power module. (b) Conventional non-baseplate power module, mounted on a 6063 aluminum alloy heatsink. (c) Conventional power module with stacked substrates.

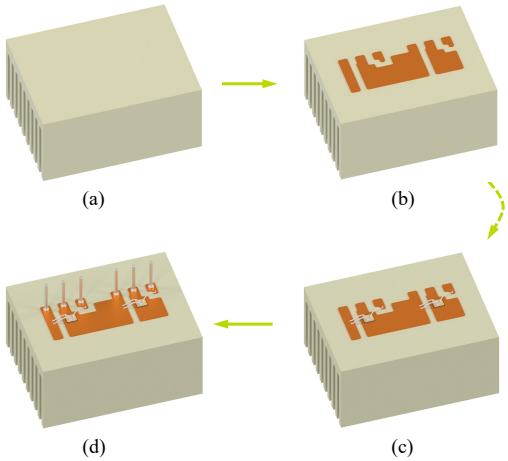
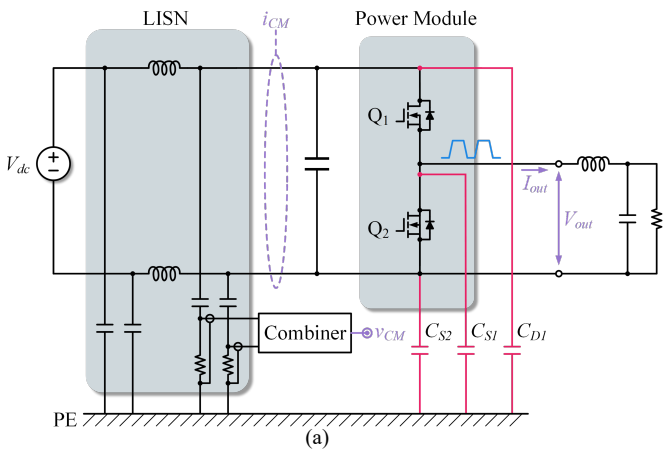


Fig. 5. Chip-on-ceramic heatsink power module manufacturing and assembly processes. (a) AlN ceramic heatsink manufacturing. (b) Metallization on the ceramic heatsink, including circuit pattern etching process. (c) Die attach and wire bonding. (d) Terminal soldering.

assembly process would require installing a plastic case and applying encapsulant to protect the devices and provide insulation. To achieve this, screw holes should be drilled on the ceramic heatsink during the manufacturing process to allow for plastic case installation. Alternatively, adhesive can be used to attach the plastic case to the ceramic heatsink, similar to most commercial non-baseplate packages.

B. Experimental Results

To experimentally characterize the EMI performance of the different types of power modules, a 400 V to 200 V buck converter is constructed. Fig. 6(a) provides the measurement schematic of the converter. The CM current i_{CM} is measured using a current probe, and the CM voltage v_{CM} from the line impedance stabilization network (LISN) is routed to a combiner, which then connects to an oscilloscope for monitoring. Additionally, the output voltage V_{out} and current I_{out} are also measured for reference purposes. Fig. 6(b) illustrates the experimental setup. The LISN model in this experiment is



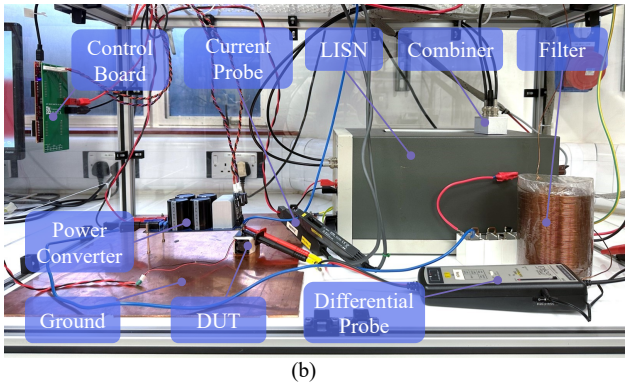


Fig. 6. Measurement of CM noise in non-isolated buck converter. (a) Schematic of the measurement circuit. (b) Experimental setup.

EMCO 3825/2 with 400 V maximum voltage rating. A copper plate is placed under the power module working as the ground.

The parasitic capacitance from the switching node to ground ($C_{O,PE}$) of the entire experimental setup, including the ceramic and conventional modules, is 29 pF and 70 pF, respectively. The parasitic capacitance of the ceramic module and conventional module alone is 4 pF and 45 pF, respectively.

Fig. 7 and Fig. 8 show the waveforms of the CM noise test results at 100 kHz and 150 kHz switching frequency, respectively. The results indicate that the CM current and voltage peaks occur during the turn-on and turn-off transients of the MOSFETs. In comparison, the EMI performance of the conventional package with stacked substrates is better than that of the conventional package with a single substrate, but it exhibits higher CM noise than the ceramic package. The ceramic package demonstrates the lowest CM noise among the three configurations, confirming that the chip-on-ceramic heatsink structure can effectively reduce CM noise.

Fig. 9(a) and Fig. 9(b) show the frequency spectrum of the CM current for the SiC buck converter at switching frequencies of 100 kHz and 150 kHz, respectively. The frequency spectrum demonstrates that, compared to the traditional package with a single substrate, the CM current of the package with stacked substrates is reduced by approximately 2 dB, while the CM current of the chip-on-heatsink package is reduced by more than 5 dB between 5 MHz and 20 MHz.

The thermal properties of the modules are characterized by the thermal resistance of junction-to-ambient $R_{th,ja}$. Fig. 10

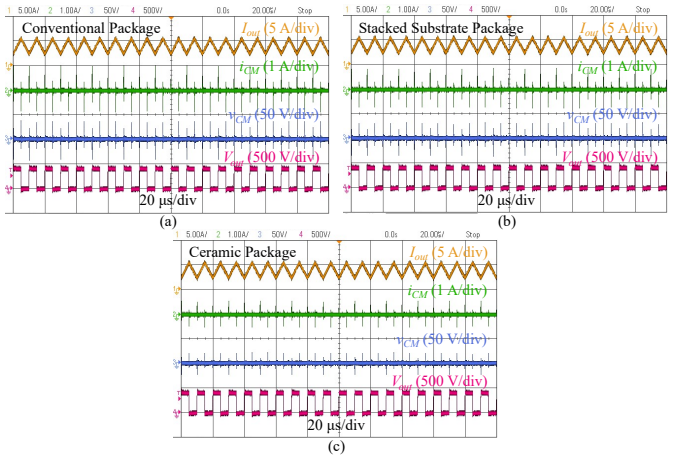


Fig. 7. Experimental result of output current I_{out}, output voltage V_{out}, CM current i_{CM}, and CM voltage v_{CM} at 400 V dc-link voltage and 100 kHz switching frequency for (a) the conventional non-baseplate power module, (b) the conventional module with stacked substrates, and (c) the chip-on-ceramic heatsink power module.

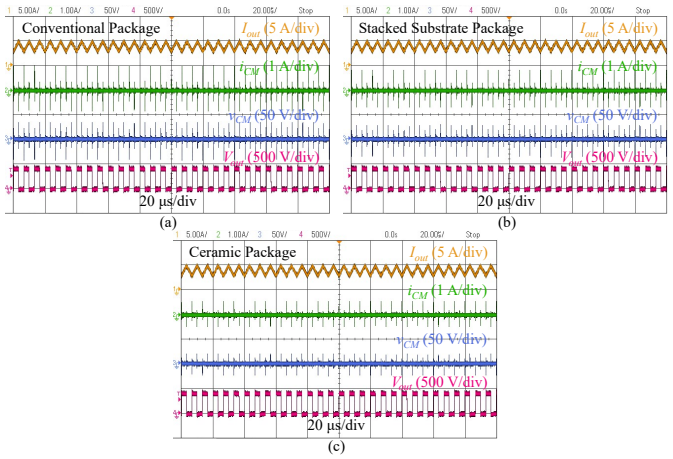


Fig. 8. Experimental result of output current I_{out}, output voltage V_{out}, CM current i_{CM}, and CM voltage v_{CM} at 400 V dc-link voltage and 150 kHz switching frequency for (a) the conventional non-baseplate power module, (b) the conventional module with stacked substrates, and (c) the chip-on-ceramic heatsink power module.

shows the thermal images captured at a total power loss of 40 W (20 W for each MOSFET) under an ambient temperature of 22.5 °C. Thermal test results indicate that the chip-on-ceramic heatsink module with the AlN heatsink exhibits better thermal performance compared to the conventional module. Specifically, the measured $R_{th,ja}$ is 1.79 °C/W for the chip-on-ceramic heatsink module and 1.82 °C/W for the conventional one, demonstrating the enhanced thermal efficiency of the chip-on-heatsink configuration.

Fig. 11 presents the computational fluid dynamics (CFD) simulation results for both the chip-on-ceramic heatsink power module and the conventional module. The simulation is performed using Ansys Icepak to calculate the temperature distribution and thermal resistance of each layer. The boundary conditions of the thermal model are consistent with the experimental conditions, with a total power loss of 40 W (20 W for each MOSFET) under an ambient temperature of 22.5 °C.

The simulation results closely match the thermal experi-

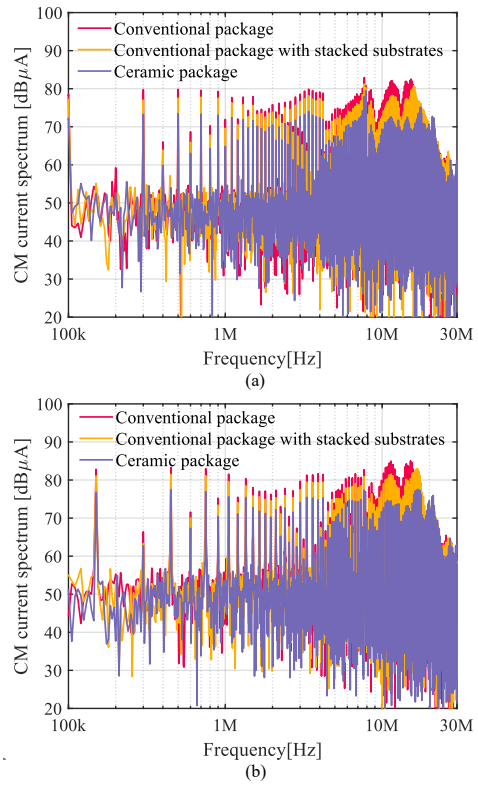


Fig. 9. Frequency spectrum of the CM current from 100 kHz to 30 MHz for three different packages at (a) 100 kHz switching frequency, and (b) 150 kHz switching frequency.

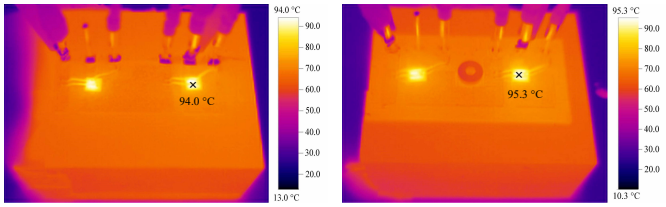


Fig. 10. Thermal test results of ceramic and conventional power modules at a total power loss of 40 W (20 W for each MOSFET) under an ambient temperature of 22.5 °C. (a) Chip-on-ceramic heatsink power module. (b) Conventional power module.

ment, illustrating the total $R_{th,ja}$ of the ceramic package is lower than that of the conventional package, at 1.79 °C/W versus 1.82 °C/W. The results also show that the heatsink-to-air thermal resistance ($R_{hs,air}$) of the AlN ceramic heatsink is higher than that of the aluminum alloy heatsink, at 1.59 °C/W versus 1.45 °C/W, respectively. This is due to the lower thermal conductivity of AlN (180 W/m°C) compared to 6063 aluminum alloy (209 W/m°C). However, the reduced number of layers between the chips and the heatsink in the chip-on-ceramic heatsink structure allows the overall $R_{th,ja}$ of the ceramic package to be lower than that of the conventional package.

IV. Remarks

In addition to its EMI and thermal performance benefits, the chip-on-ceramic heatsink package can introduce other

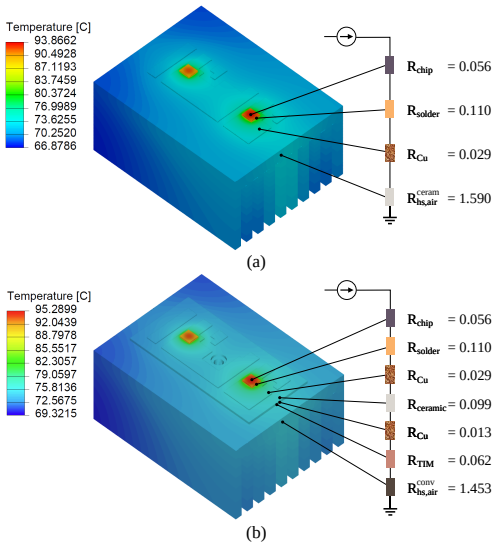


Fig. 11. Simulation results of temperature field distribution and thermal resistance of each layer for (a) chip-on-ceramic heatsink and (b) conventional power modules.

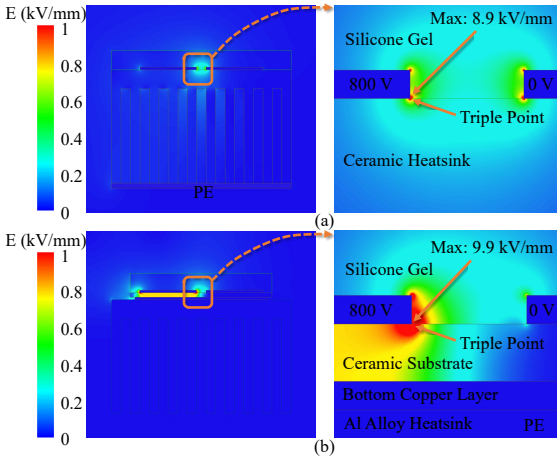


Fig. 12. Simulation results of 2D electric field distribution. (a) Chip-on-ceramic heatsink power module. (b) Conventional power module.

advantages and potential disadvantages to the power electronic system. These aspects should be carefully considered during the application of this package structure.

A. Reducing the Risk of Partial Discharge

Fig. 12 illustrates the 2D electric field distribution for both the ceramic and conventional packages at 800 V dc voltage. It can be seen that for the ceramic package, an additional electric field is introduced around the ceramic heatsink. However, the strength of this field is nearly two orders of magnitude lower than the maximum electric field, which occurs at the triple point of the module. Additionally, the zoomed-in view reveals that the electric field at the triple point of the chip-on-ceramic heatsink module is lower than that of the conventional module, potentially reducing the risk of partial discharge in the module.

B. No Need Grounding

As shown in Fig. 6(b), the ceramic heatsink of the module sits on a copper plate for CM noise measurement. In prac-

tical applications of power modules with ceramic heatsinks, grounding the ceramic heatsink is not necessary. While metallic heatsinks in conventional designs must be earthed for safety reasons when exposed outside the chassis of a power electronic system, ceramic heatsinks, due to their insulating properties, can be safely exposed without the need for grounding.

C. Improve the Power Density

Using ceramic package can enhance EMI performance, thereby lowering filtering requirements and allowing for a smaller filter size. The ceramic package also reduces the number of layers in the module, enabling a more compact layout. As a result, the overall power density of power electronic systems can be improved with chip-on-ceramic heatsink power modules.

D. Brittleness and Cost

Ceramic materials are characterized by their brittleness. This inherent brittleness makes them vulnerable to rupture, particularly under impulsive loading conditions. Therefore, it is crucial to design ceramic heatsinks with careful consideration to enhance their impact strength and toughness, ensuring that the ceramics remain within their elastic region throughout assembly and operation to prevent structural failures. Another drawback of ceramic heatsinks is their cost. Currently, ceramic heatsinks are more expensive than aluminum alloy heatsinks. In practical applications, it is important to strike a balance between performance and cost.

V. Conclusion

This letter proposes the use of a chip-on-ceramic heatsink power module structure to reduce CM noise in power converters. By directly attaching SiC MOSFETs to metallized AlN ceramic heatsinks, this design eliminates the necessity for traditional substrates and metal heatsinks, thereby significantly reducing parasitic capacitance between conductive traces and the ground. The effectiveness of this configuration has been verified through comparative experiments involving different types of power modules, including the chip-on-ceramic heatsink module, a conventional module, and a conventional module with stacked substrates. EMI analysis is conducted using a 400 V to 200 V DC-DC buck converter, and the results confirmed that the chip-on-ceramic heatsink configuration achieves a reduction in CM noise, with more than 5 dB decrease in CM current between 5 MHz and 20 MHz compared to the conventional non-baseplate power module package. Additionally, thermal test results indicate that the chip-on-ceramic heatsink module exhibits better thermal performance compared to the conventional module, due to the reduced layers between the heatsink and dice. These findings demonstrate the potential of the chip-on-ceramic heatsink structure to effectively mitigate CM noise in power converters, providing a substantial improvement over traditional designs and offering a promising solution for enhancing the EMI performance of power electronic systems.

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