Influence of thermal processing on the electrical characteristics of MOS capacitors on strained-silicon substrates

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Oxidation of very low energy nitrogen–implanted strained-silicon

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Abstract

In the present work we perform a systematic study of oxidation of very low energy nitrogen implanted strained silicon in terms of oxide growth, structural characterization of the implanted strained silicon substrate and electrical properties of the ultra thin oxides as a function of the substrate strain level. Low energy (3keV) nitrogen ($N_2^+$) implantation was performed in strained-Si/SiGe/Si substrates of various strain levels and oxidations were carried out for different times at 850°C. It has been found that nitrogen implantation efficiently blocks silicon oxidation, independently of the strain level of the substrate. TEM analysis revealed the full absence of extended defects in the strained silicon substrate after the thermal treatments. The grown oxides exhibit very good electrical properties in terms of interface trap densities and leakage currents.

\textbf{Keywords:} Strained Silicon, Nitrogen, Ion implantation, Oxidation, Metal-oxide-semiconductor structures, Electrical measurements

1. Introduction

Semiconductor technology has reached a point where the physical dimensions of the devices pose a barrier to device scaling. There has been a great gain of momentum in the development of composite substrates as an alternative way of increasing device performance without further shrinking of the device, the most important of which is strained-Silicon. Strained-Si pseudomorphically grown on relaxed SiGe virtual substrates can provide higher mobility for both electrons and holes [1,2]. The strained silicon layer is tensile, since the lattice constant of the Si$_x$Ge$_{1-x}$ layer is greater than that of Si. The tensile strain breaks the degeneracy of the Si conduction band so that only two valleys are occupied instead of six. This conduction band split results in a very high in-plane mobility in the strained-Si layer (>2900 cm$^2$/V s with electron densities of about $10^{12}–10^{13}$/cm$^2$ and closer to 1000 cm$^2$/V s with hole densities $>10^{12}$/cm$^2$). By using the high mobility strained-Si as the channel region in a metal oxide semiconductor field-effect transistor (MOSFET), the device speed can be improved substantially without further shrinking of the device [3].

In parallel, as the dimensions of modern electron devices decrease, the need for even thinner and reliable gate dielectrics becomes more demanding. Standard Silicon oxidation in nitrogen – rich ambient has been established as an important method of fabricating highly reliable ultrathin (< 4nm) gate oxides [4]. Oxidation of nitrogen - implanted silicon is one of the physical methods developed in order to incorporate nitrogen within the growing oxide. The method makes use of the non-Fickian behavior of nitrogen diffusion towards the surface during annealing, the mechanism of which is still under investigation. During the temperature ramping of the oxidation process, nitrogen moves toward the surface and penetrates the growing oxide layer after segregating at the Si / SiO$_2$ interface. The method offers two main advantages:

(a) The incorporation of a controllable large amount of nitrogen within the oxide is attainable by properly varying the implantation dose, avoiding the complex chemistry of the chemical methods such as nitrous oxidation (in NO ambient) and oxynitridation (in N$_2$O ambient).

(b) It enables the formation of various oxide thicknesses across the Silicon substrate by performing local nitrogen implantations of various dose and using one single oxidation step, which is very useful for Systems On Chip fabrication.

The main disadvantage of the method was the formation of implantation – induced extended defects in the silicon substrate for medium energy range (25 – 40 keV) nitrogen implantations. Recently it has been demonstrated [5,6,7] that the use of very low energy (<10 keV) – high dose ($10^{13}$ cm$^{-2}$) $N_2^+$ implantation can lead to the formation of highly reliable ultrathin (< 4nm) gate oxides on extended defect – free silicon substrates which exhibit superior electrical properties as compared to the corresponding formed using medium energy (25-150 keV) implantation.

The purpose of this work is to study oxidation of very low energy nitrogen – implanted strained–Silicon in terms of the dependence of the oxide growth on strain level,
the defect characterisation of the strained Silicon substrate and of the electrical properties of the oxides.

2. Experimental

Three sets of substrates were examined in this work. These were denoted as S0, S1 and S2. Substrate S1 has a strained silicon layer of 27.5 nm on top of a constant composition SiGe layer with 10% Ge content, which is on top of a graded layer of SiGe, in which the Germanium content increases linearly to 10%. Substrate S2 has a strained layer of 13 nm on top of a constant composition SiGe layer with 20% Ge content, which is on top of a graded layer of SiGe that reaches a Germanium content of 20%. On both samples, the underlying substrate is a p-type epi layer on p++ substrate wafer as shown in Figure 1.

The strained silicon wafers were provided by MEMC Electronic Materials Inc. Substrate S0 is a standard p-type Czochralski silicon wafer, which was used as a reference. Very low energy (3 keV) – high dose (10^15 cm^-2) N_2^+ implantation was performed on all substrates. The nitrogen - implanted samples were named S0N, S1N and S2N respectively. Oxidations have been performed at 850°C for three different oxidation times (30, 60 and 120 min respectively). After removal of the backside oxide, aluminum was evaporated on both sides of the samples through an electron-beam evaporation system and photolithographically patterned to form MOS capacitors with 1x10^-4 cm^-2 and 4x10^-4 cm^-2 gate area. All samples were subjected to forming gas annealing at 380 °C for 20 min. Transmission Electron Microscopy was used to reveal the presence of extended defects in the strained – Silicon overlayer after oxidation. The electrical characteristics of the oxides have been studied using bias and frequency dependent capacitance (C–f, C–V) and conductance (G–f, G–V) measurements, as well as I–V measurements at room temperature.

3. Results and discussion

3.1 Oxide growth study

Oxide growth study was performed in order to reveal the influence of substrate strain level on nitrogen diffusion towards the surface and consequently on oxidation rate. The thicknesses of the oxides formed at various time intervals (30 min, 60 min and 120 min) were measured by means of ellipsometry and electrical measurements. Since the oxides are ultrathin, their thicknesses cannot be calculated from the accumulation capacitance, which overestimates thin oxide thickness. Therefore, the method proposed by Maserjian was employed for the extraction of the electrical oxide thickness from C-V measurements [8,9]. Very good agreement was found between the physical oxide thickness measured directly by ellipsometry (assuming a refractive index of 1.46) and the electrical oxide thickness extracted from the C-V measurements. All implanted samples showed oxide thickness in the 2 nm – 2.7 nm regime. The oxide thickness as a function of time and substrate strain level is plotted in Figure 2(a). The corresponding thicknesses of non-implanted reference samples (S0, S1 and S2) are shown in Figure 2(b).

For the non-implanted samples the oxidation rate does not depend, within experimental error, on the substrate strain level in agreement with previous experimental results [10, 11]. For the nitrogen implanted samples, similar oxide thickness reduction was measured for all samples, independent of the strain level, indicating that strain does not affect significantly the diffusion of nitrogen towards the surface. There is evidence [12, 13] that nitrogen in silicon diffuses towards the surface via an interstitial – mediated mechanism using the interstitial supersaturation induced by the implantation or oxidation process. Moreover, it has been demonstrated [14] that the presence of a pressure field in the silicon substrate affects the equilibrium and non – equilibrium point defect population. Therefore, nitrogen diffusion towards the surface may depend on the substrate strain level. However, such dependence has not been observed for the present experimental conditions and is a matter that requires further investigation.

![Figure 1. Experimental structures.](image-url)
3.2 Substrate characterization
In a previous work [5], it has been demonstrated that low energy N⁺ (3 keV) implantation at a relatively high dose (10¹⁵ cm⁻²) leads to thin oxides with improved electrical characteristics, while a total absence of extended defects had been observed [6,7]. In this work, the aforementioned results have been confirmed for the case of strained – silicon substrates as well, by extended TEM analysis. Figure 3 illustrates a TEM cross section for the particular case of sample S1N where a complete absence of extended defects is observed. It is well known that during the annealing step which follows an amorphizing implant in silicon, a layer of extrinsic (interstitial-type) dislocation loops is created in the vicinity of the former amorphous/crystalline interface. In our case, the absence of extended defects in the strained – silicon substrate can be attributed to: a) the proximity of the SiO₂/Si interface to the layer of extended defects, since the presence of a SiO₂/Si interface close to an extended defect population acts as an interstitial sink leading to the defect band dissolution [15] and b) to the tensile strain of the substrate since it has been demonstrated that under the presence of a tensile pressure field a fast dissolution of an extrinsic type extended defects population during annealing takes place [14].

3.3 Electrical Properties of the oxides
Fig. 4 shows typical high-frequency Capacitance-Voltage characteristics performed within the frequency range of 1 MHz to 1.6 kHz of sample S1N grown at 850 °C for 30 min (after post metallization annealing). The C-V measurements showed no evidence of dispersion at the accumulation or inversion region indicating the absence of strong leakage currents. In double sweep measurements between inversion and accumulation, a small hysteresis loop of 10 mV appears. At frequencies lower than 1MHz, dispersion at the depletion region is evident due to the response of the residual interface traps, which remain after the post-metallization annealing treatment. The flat-band voltage was determined to be -0.7V. The oxide thickness was estimated from the Maserjian capacitance method and found to be very close to 2 nm. The density of fixed charges was determined to be 5x10¹² cm⁻². The evaluation of the density of interface traps was performed by the Gp/ω versus frequency curves assuming the approximate expression: Dₜ ≈ 2.5/q (Gp/ω)max. The densities of interface traps, near midgap, extracted by this method are shown in Table I for all samples. These were found between 4.7 x 10¹⁰ eV⁻¹cm⁻² to 9.7 x 10¹⁰ eV⁻¹cm⁻² and seem to decrease for increasing oxidation time. A typical Gp/ω versus frequency curve is
shown in Fig. 5. Additionally, I-V measurements (not shown) exhibit breakdown fields of around 11-12 MV/cm. Finally, strained-silicon samples exhibit leakage currents, for gate injection, an order of magnitude higher than that of the reference sample S0N. In general, nitrogen implanted samples exhibit satisfying properties and meet the typical requirements needed for a good quality gate dielectric of this thickness.

4. Conclusions
It is therefore possible to produce ultrathin oxides with a low density of interface states by oxidizing low energy nitrogen – implanted strained silicon substrates. The effect of strain level on the out-diffusion of nitrogen, if any, did not have an effect on the oxide growth rate, enabling the formation of good quality thin oxides even with high thermal budget. On the other hand, low-energy nitrogen implantation does not show any extended defects in the implanted strain silicon substrate, thus making this technique promising.

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