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TURN-OFF FAILURE MECHANISM IN LARGE AREA IGCTS

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Abstract *– The destruction mechanism in large area IGCTs (Integrated Gate Commutated Thyristors) under inductive switching conditions is analyzed in detail. The three-dimensional nature of the turn-off process in a 91mm diameter wafer is simulated with a two-dimensional representation. Simulation results show that the final destruction is caused by the uneven dynamic avalanche current distribution across the wafer.*

Keywords: *Large Area SOA, Integrated Gate Commutated Turn-off Thyristor.*

1. INTRODUCTION

IGCTs feature the most competitive trade-offs in the very high power range of the Power Semiconductor Device spectrum. At high current densities, they offer excellent reliability, lower conduction losses and larger utilization of silicon area than any other high power semiconductor devices such as IGBTs, GTOs or Light Trigger Thyristors. IGCTs also meet the device requirements of high-power converters for a future DC distribution system which will be required to handle an increasing share of renewable power. [1;2;3]

One of the biggest challenges in the further development of IGCTs is the increase of the maximum controllable current (MCC) density in large area IGCTs. Indeed, although the MCC increases with increasing active area, the MCC density decreases with increasing active area and until today none of the suggested techniques [4;5;6;7] gives a perfect linear scaling law.

Even though there has been a great effort to understand the failure mode in IGCTs during turn-off, there is no detailed description and analysis of this phenomenon. In light of the increasing importance of IGCT devices, this paper aims to provide a detailed explanation for the failure mechanism under inductive turn-off in a standard large area IGCT device.

2. METHOD

A GCT wafer is made up of a large number of parallel connected cells arranged in concentric rings. These are controlled by a single gate contact as illustrated in Fig.1. The cell structure and doping design is illustrated in Fig.2.

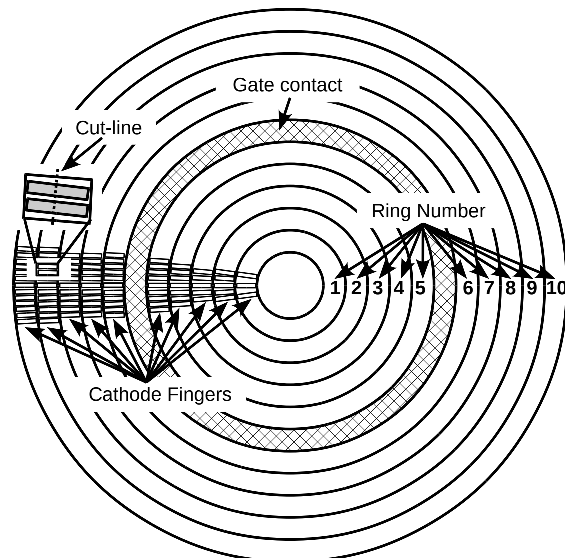


Fig. 1 A 91 mm diameter GCT Wafer with gate contact in the middle of the wafer. More than 2700 cells are connected in parallel.

The large geometry introduces an imbalanced inductive loading between the cells positioned in different rings. The cells farther from the gate contact have an increased stray gate inductance and lag behind in the turn-off process. The inductance of the individual segment rings on a GCT wafer is reported in [4].

The representation of the heavy cell paralleling has been addressed by performing

two-dimensional simulations on two physically defined GCT structures connected in parallel in a SPICE defined external circuit. All simulations are isothermal (400 K). The SPICE circuit used for the simulations throughout this paper is shown in Fig. 3.

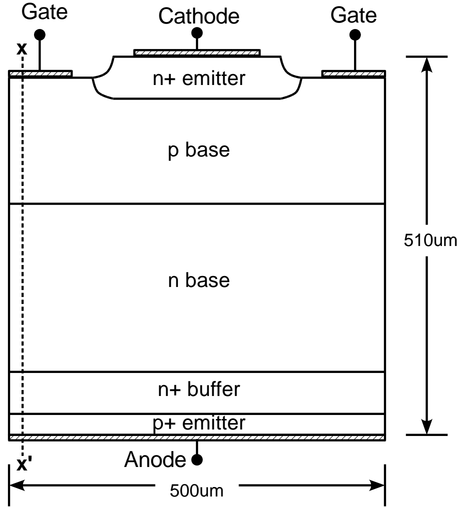


Fig. 2 The structure and doping design of a conventional GCT cell (Cut-line indicated in Fig.1)

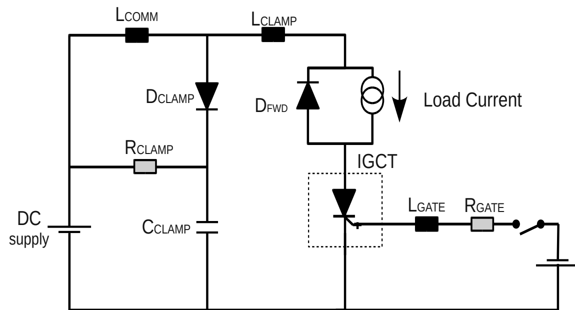


Fig. 3 The circuit used for simulations throughout this paper

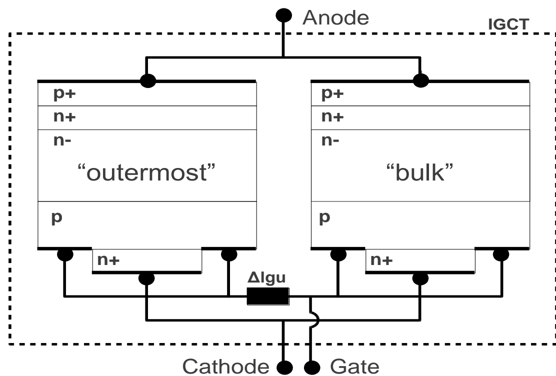


Fig. 4 Simulation method: Simulation of two cells connected in parallel to model the bulk ("bulk") region of the device and the region to turn-off last ("outermost"). Δl_{gu} corresponds to the increased gate inductance of the outermost region-gate.

In the simulation arrangement shown in Fig. 4, the GCT labeled "bulk" represents the rings 1 to 9 which account for about 80% of the device active area. The one labeled "outermost" represents the outermost 20% of the active area (ring 10) which is the region that turns-off last. It features an increased gate inductance equal to Δl_{gu} relative to the bulk device area. This perturbation allows for a realistic representation of the three dimensional nature of the turn off process in a GCT device with a two-dimensional simulation. Similar simulation arrangements have been used in [5] and [8].

Sentaurus Structure Editor has been used to create the physical representation of the GCT cells and Sentaurus Device to apply the simulations.

3. RESULTS

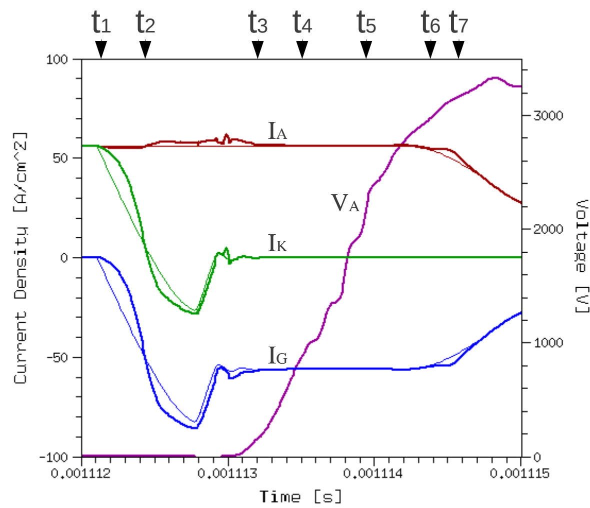
Fig. 5(a) shows the simulated last pass turn off waveform. Under on-state conditions the current density is uniform throughout the device. The turn off initiates at time instance t_1, with the application of negative potential on the device gate contact. This in turn starts the extraction of the holes from the p-base of the device.

The increased gate inductance of the outermost region with respect to the bulk region of the device decreases the rate at which the anode current commutes from the cathode to the gate. Therefore the extraction of plasma from the p-base is slower in the outermost region during the first moments of the turn-off phase. Inevitably this causes a local increase in the current density (t_2).

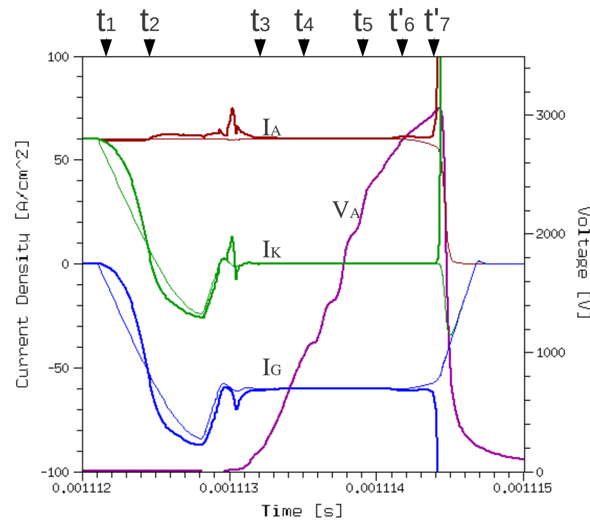
The cathode/p-base junction becomes reverse biased before any space charge in the main junction starts forming. This isolates the n+ emitter and ensures that conditions of the hard drive regime are fulfilled. At t_3, the whole of the anode current is commutated from the cathode to the gate contact of the individual cells and the voltage rise phase starts. The outermost region enters this phase with a slightly higher current density compared to the bulk region.

The rate of voltage rise starts to decrease at t_5 because of an increasing carrier multiplication effect in the depletion region. This can be identified in the waveform by the characteristic "knee" in the anode voltage. At t_6, the anode voltage reaches the operating voltage V_D and the

current starts to commutate from the IGCT to the free-wheeling diode. As shown in Fig. 5(a), the outermost region resists this change until t_7.



(a) Last Pass Turn Off Waveform



(b) Turn Off Failure Waveform

Fig. 5 Comparison of the turn off in the "bulk" region (thin solid lines) and the "outermost" region (thick solid lines) of the device at T=400 K, V_{DC}=2.8 kV, L_{COMM}=3 µH, C_{CLAMP}=10 µF, L_{CLAMP}=0.3 µH

By keeping the same operating conditions but increasing the conduction current above SOA the device fails to turn off. The turn-off failure waveform is shown in Fig. 5(b). In this case, there is a considerable increase in the anode current density of the outermost region after t'_6. As shown in Fig. 6, the density of charge carriers is higher in the outermost region than in the bulk. The resistance of the outermost region is consequently reduced, which enhances this current redistribution effect. At t'_7, the anode current density in the outermost region increases dramatically. This in turn forward biases the cathode which starts to emit, and the voltage collapses.

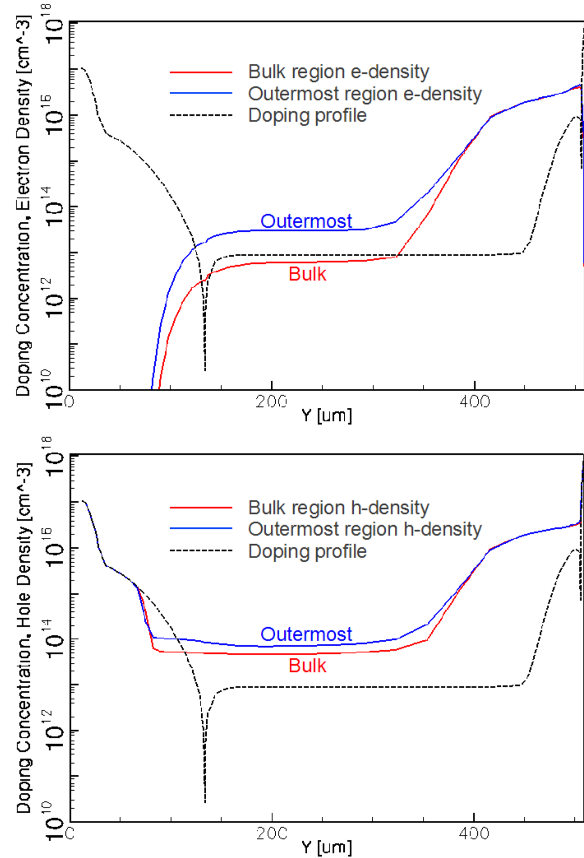


Fig. 6 Electron - Hole and Doping distribution of the outermost and bulk regions (along x-x' in Fig. 2) at t'7

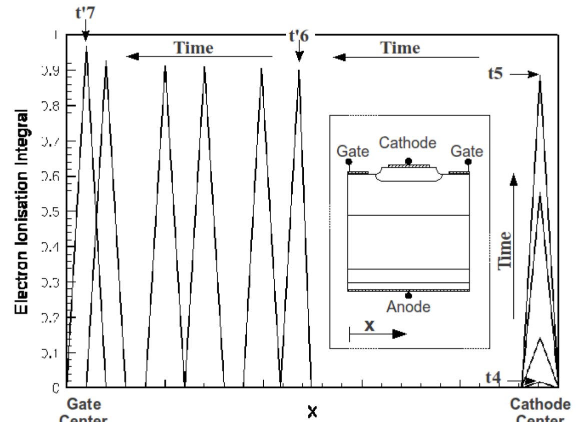


Fig. 7 The evolution and the spatial propagation of the Electron Ionization Integral during turn off in the outermost region of an IGCT device.

At the moment of destruction (t'_7) the electron ionization integral in the outermost region approaches unity (Fig. 7). Simulation results have shown that the hole ionization integral at the same time instance is about ten times smaller. As shown in Fig. 7, the peak impact ionization effect

develops under the center of the cathode and propagates towards the region below center of the gate during the turn-off.

4. DISCUSSION

The most important feature of an IGCT is the transformation of the regenerative p-n-p-n thyristor structure in a p-n-p transistor structure prior to the formation of any space charge in the main blocking junction. This means that during turn-off, thousands of p-n-p transistors are connected in parallel in an IGCT wafer.

During the storage phase of the turn-off, there is an initial current redistribution of the conduction current from the cells closer to the gate contact to those who are farther away. This current redistribution happens at low voltage and it is not destructive. The cells in the outermost region however, continue to carry a slightly higher current share throughout the voltage rise phase.

By the end of the voltage rise phase, the device still conducts full current and the potential across it is close to the supply voltage (V_{DC}). Under these conditions, the dynamic avalanche effects become important. The carrier generation in the space charge region of the device creates an electron current that adds up to the base current of the p-n-p transistor structure. The pre-existing condition in the outermost region of a slightly increased current density enhances the avalanche phenomena locally.

Towards the end of the voltage rise period the whole anode current is carried by the gate. This gives rise to an increased current density in the proximity of the gate p-base region compared to the p-base region below the cathode. Thus the impact ionization effect in this region is enhanced. When the electron ionization integral becomes close to unity, the electron current is considerable. The additional local electron current drives the p-n-p transistor of the outermost region. Beyond the maximum controllable current, the resulting collector current of the p-n-p transistor is large enough to forward bias the n+p junction of the main thyristor in the outermost region; thus the device will latch up. This local effect leads to the destruction of the device.

5. CONCLUSIONS

The three-dimensional nature of the turn-off process in large diameter IGCTs was simulated with a two-dimensional model. The model depicts the current redistribution effects due to the imbalanced gate inductive loading in large diameter wafers and explains the origin of the device failure in high current inductive turn-off conditions. For the first time the failure of the device is linked with the spatial movement of the electron impact ionization region and the local re-triggering of the p-n-p structure of the outermost cells. This work enhances our understanding of the physics in the device at the destruction moment. An improved three-dimensional model is currently under study.

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