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The Destruction Mechanism in GCTs

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Abstract—This paper focuses on the causes that lead to the final destruction in standard Gate Commutated Thyristor devices (GCTs). A new 3D model approach has been used for simulating the GCT which provides a deep insight into the operation of the GCT in extreme conditions. This allows drawing some conclusions on the complex mechanisms that drive these devices to destruction, previously impossible to explain using 2D models.

Index Terms— Full Wafer Modeling, Gate Commutated Thyristor, GCT, Maximum Controllable Current, MCC, Safe Operating Area, SOA, Thyristor.

I. INTRODUCTION

THE need for increased controllability in bipolar devices has been the subject of research for many years with some early improvements coming from the use of field controlled gate patterns in p-i-n diodes and thyristors [1,2]. There was also a strong effort to include MOS controllability in turn-off thyristors [3,4]. In Gate Turn Off thyristors (GTOs) the main improvements have been made by improving the gate units [5,6]. The latter paved the road for the introduction in 1997 of the Integrated Gate Commutated Thyristor (IGCT) [7], the most efficient and economical solution of all. It is now the power device of choice for many high power applications with its market share increasing continuously mainly because of the application-specific performance tailoring of the device but also due to the increased SOA and the expansion of its operation at higher temperatures [8,9]. The main features of this device are: (i) the low on-state losses due to its latching nature, (ii) the possibility of scaling up in current to thousands of amperes and (iii) the good ruggedness. The state-of-the-art GCT design is based on cathode islands surrounded by the gate metallization. Unlike the GTO, the GCT can be turned-off in a ‘pure’ transistor mode, by taking out all the current via the gate. The gate/cathode interdigitation density is very high, to allow safe removal of the entire anode current during the switch-off period, without the risk to re-ignite the thyristor. The GCT is thus based on the principle that latching devices are best for on-state conduction while the transistor (rather than the thyristor) turn-off is safer and faster. Another important aspect of GCTs, when compared to GTOs is that

they no longer need snubbers, reducing the component count which ultimately increases the reliability. The current research focuses on enhancing the current that can be fed into a single wafer by either increasing the device dimensions or by increasing the Maximum Controllable Current (MCC) density. At the same time, we aim to improve the high temperature device performance (junction temperature T_J to 400K and above). The challenge in achieving this arises from the already large dimensions and the strong parallelization within the wafer. Experimental and simulation work show an uneven current sharing in the device at the onset of turn-off. The origins of this peculiarity have been traced in the parasitic unequal distribution of inductances and resistances of the gate metallization network [8,10,11].

II. PROCEDURE FOR SINGLE WAFER DEVICE SIMULATIONS

Method of investigation – Modeling the GCT – Test circuit

The GCT is a wafer device and as such, its detailed simulation is difficult. From various device observations, and destructive experiments, it has been observed that these large devices are prone to large current redistribution during the turn off process. Previous studies on GCTs have shown that the inductive loading within the wafer is not uniformly distributed. It has been found that sections of the device closer to the gate contact experience lower inductance during turn-off compared to those farther from it. The impedance loading along a radial line extending from the center of the wafer was reported in [8]. This imbalance alongside with the geometrical features of the wafer device strongly perturbate the turn-off procedure thus in order to reproduce the behavior of the GCT in dynamic conditions, the interaction between adjoining regions in the wafer has to be taken into account in a simulation model.

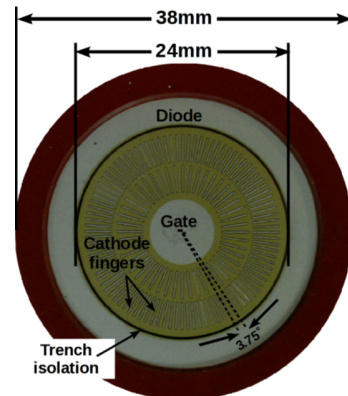


Fig. 1. 38mm Reverse-Conducting IGCT wafer

The traditional device models are two-dimensional, assuming uniformity in the third dimension. With symmetry, one can extract a minimum amount of information. Various arrangements exist for these devices. A three-dimensional model for full wafer devices has only recently been introduced

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by us [12]. The high complexity and demand in computational power and memory made this previously impossible. Such a model is expected to give a more accurate prediction of the absolute value of the MCC compared to that resulting from the two-dimensional counterpart. This is because a full wafer 3D model takes into consideration all the geometrical and physical features of the wafer and it can capture current and space charge traveling via silicon from one GCT cell to another.

In this work we used 4.5kV reverse-conducting IGCTs fabricated by ABB with a diameter of 38mm shown in Fig. 1. The GCT part of the device has an active area of 3.5cm^2 and diameter of 24mm. This GCT device features two rings of cathode segments. These long and narrow cathode segments are surrounded by the gate metallization which forms the gate contact in the middle of the wafer. For finding out the MCC of this device MCC in inductive switching we used the test circuit shown in Fig. 2. It has a di/dt and an over-voltage clamp but no dV/dt snubbers and it aims to mimic with a high degree of accuracy the operation in standard applications i.e. inverter circuits or choppers.

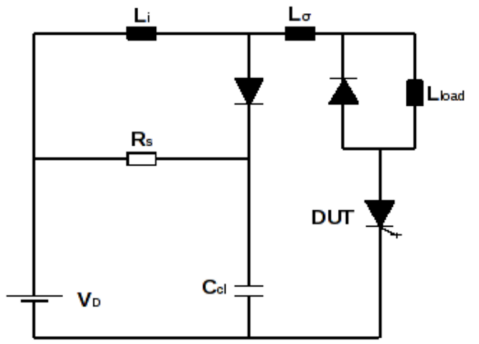


Fig. 2. The external circuit used for MCC measurements.
di/dt Limiting Inductor $L_i=25\mu\text{H}$, Clamp Capacitor $C_{cl}=0.5\mu\text{F}$, Stray Inductance $L_\sigma=1\mu\text{H}$, Damping Resistor $R_s=4.2\Omega$

2D Models

In the 2D approach, the wafer is split in regions which are modeled by separate (or connected) numerical devices. Then particular perturbations are applied to these regions to extract information about what happens when a region deviates from the expected behavior due to the introduced instability. Fig. 3 illustrates the traditional model approach [13,14] of the GCT as used for this study. Indeed it is a mixed mode representation with a combination of numerical devices and SPICE components. This model of parallel connected cells assumes symmetry with fixed cathode-gate interdigitation. It consists of two numerical unit GCT cells with individual cathode, anode and gate electrodes. One cell represents the region in the device that turns off last whereas the other one represents the bulk of the device. The respective cell electrodes are connected together via a SPICE circuit which makes up for the electrical coupling in the wafer. Important aspects such as thermal interaction, current and space charge traveling from one cell to the other via the semiconductor are thus ignored. This model however accounts for the unequal spread of the parasitic inductances and resistances due to the

gate metallization. These parasitics are modeled by a network of resistances and inductances which introduce uneven delays in the turn-off signal between two distinctive regions in the GCT wafer device, the one closer to the gate contact and the one farther from it. These unit cells are identical in doping profile and 2D geometry and only scaled up in the “third” dimension to make up for the approximate area of the equivalent wafer region that they represent.

Such an arrangement can be set to study the effect of particular perturbations in the device like the increased inductance or resistance seen by the remotest regions of the wafer or for example the amount of acceptable variability in the doping profile etc. By assuming that the bulk of the device operates flawlessly and uniformly, the effects of the perturbation on a specific region of the device can be isolated and studied.

Also a distributed cells model exists where a number of cells connected together represent the active area of each one of the rings of cathodes that can be found in a GCT wafer (two in our case) [11,15]. In the limit for maximum 2D complexity and accuracy, every single one GCT cell is represented by one numerical device. This requires the SPICE interconnections of hundreds or thousands of numerical two dimensional GCTs.

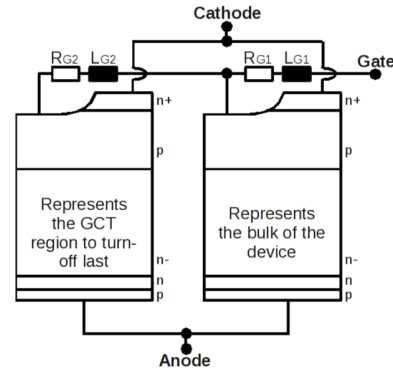


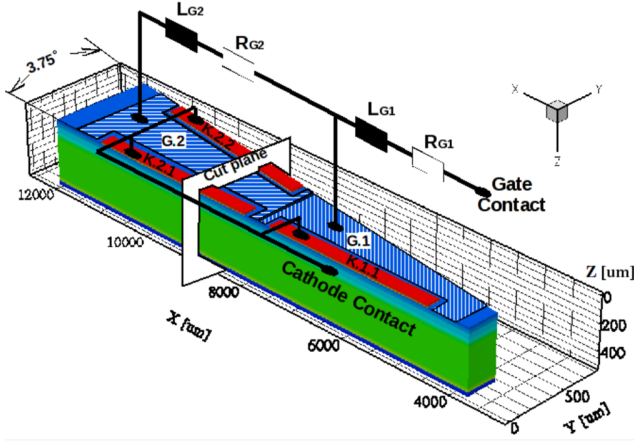
Fig.3. Traditional 2D model with parasitic gate resistance (R_{G1} , R_{G2}) and inductance (L_{G1} , L_{G2}) for wafer simulations
 $R_{G1}=0.65\text{m}\Omega$, $L_{G1}=0.4\text{nH}$, $R_{G2}=0.88\text{m}\Omega$, $L_{G2}=0.6\text{nH}$

3D Model

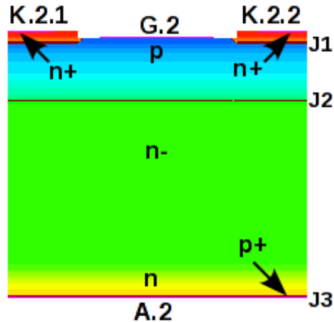
Fig. 4 shows the 3D model which is identical in 3D dimensions and physical profile to the GCT region of the 38mm in diameter Reverse-Conducting GCT shown in Fig. 1. The device dimensions for this GCT are at least three orders of magnitude larger than those in conventional 3D MOSFET or IGBT cells which makes it very demanding in memory and computational power. Furthermore, it is challenging to transfer the wafer geometrical complications into a valid 3D numerical structure with an optimized number of meshpoints.

The simulation domain used in this 3D model addresses the problem of absence of symmetry in the third dimension. As shown in Fig. 4, the gate electrode is split into two concentric regions, each one surrounding the cathode segments of the equivalent concentric ring. This split-gate arrangement allows introducing a network of SPICE resistances and inductances which account for the varying inductance-resistance formed on the metallization within the gate region of the wafer device.

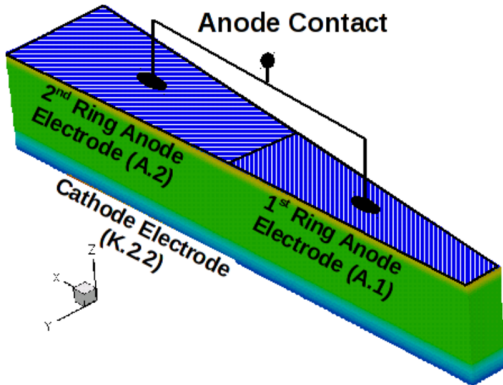
Similarly the anode electrode on the bottom side of the angular slice is also split into two regions. These two regions are however connected to the same SPICE node making up the Anode contact. By having two individual electrodes, one to cover the anode area of the inner ring and another one to cover the outermost anode ring region, the model gives a quick way to get readings of the anode current in the first and second ring without having to extract it from the numerical device. The cathode segments are also shorted together on one SPICE node which makes up for the cathode contact of the GCT.



(a) Cathode side up



(b) Device structure along the cut plane



(c) Anode side up

Fig 4. An angular slice of 3.75° of the 3D simulation domain with parasitic gate resistance ($R_{G1}=0.65m\Omega$, $R_{G2}=0.85m\Omega$) and inductance ($L_{G1}=0.4nH$, $L_{G2}=0.6nH$)

III. MCCPREDICTION AND FAILURE ANALYSIS

The calculation of the maximum controllable current requires many mixed mode simulations. This is because one simulation can only predict whether the device is able to switch off or not. For every DC link voltage (V_D) the junction temperature (T_J) is fixed to 115°C, the circuit components are kept constant and every simulation is done at different current levels to investigate the turn-off behavior. Every successful turn-off is followed by another turn-off simulation with increased current level until an MCC failure is recorded.

Successful turn-off. Here, a turn-off is considered to be successful when the anode current reduces to the typically low value of leakage current under forward blocking right after the tail phase.

MCC Failure. The GCT is considered to have failed the MCC test when during the anode voltage rise period one or more cathode segments start conducting more than 10% of the on-state anode current value.

2D Vs 3D models

The MCC was determined both with the two-dimensional model of Fig. 3 and the three-dimensional full wafer model as shown in Fig. 4. Fig. 5 shows the results of the MCC simulations as derived with the two simulation models overlaid on the experimental observations. As shown, the 3D model is able to switch off a current close to the experimental whereas the 2D model gives an overestimated MCC result because it prevents the device simulation from those 3D effects (summarized below) leading to a failure. This justifies the use of such complicated large 3D numerical structures for dynamic turn-off studies, failure analysis and device design and optimization.

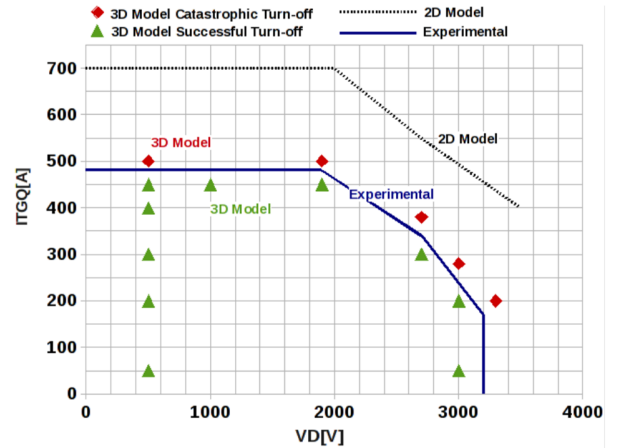


Fig. 5. The turn off current controllability ITGQ at supply voltage V_D

In summary, the two dimensional model:

1. Assumes Symmetry.
2. Assumes fixed Gate Cathode interdigitation.
3. Uses 2D numerical GCT regions.
4. Electrical coupling is made by SPICE cable connections.
5. Includes parasitic gate metallization resistance and inductance.
6. It cannot reproduce the electrical or thermal interaction or space charge moving in the third dimension within the silicon.

Advantages of the 3D model:

1. It naturally reproduces the interaction between different areas inside the device. It can hence model precisely the electrothermal interaction within the device.
2. The exact geometrical and physical features of the wafer are considered. It is an accurate 3D reproduction of dimensions and physical profile.

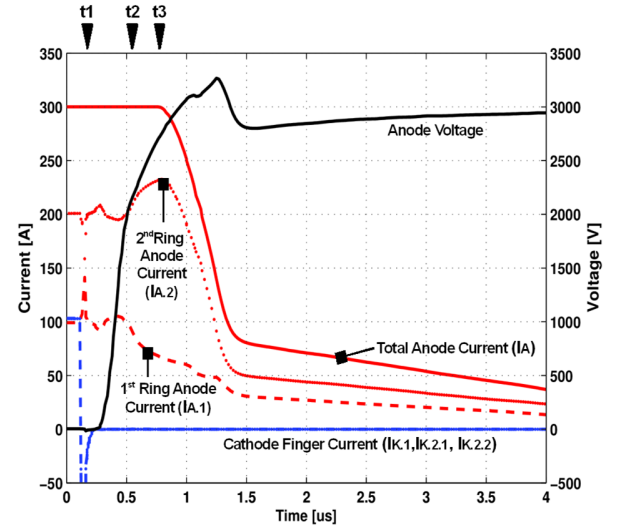
Challenges in the 3D model:

1. It is at least three orders of magnitude larger in volume than conventional 3D MOSFET or IGBT numerical cells.
2. There is additional work in transferring the complex geometric features into a valid 3D numerical structure with an optimized number of mesh points.
3. The memory and computing power requirements are very large.

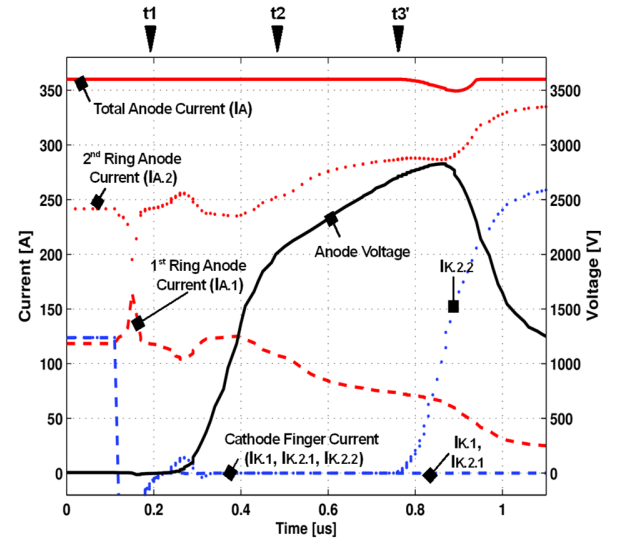
The turn-off failure

In the on-state, the conduction current is shared among the GCT segments of the model according to their active area (the effect of the parasitic resistances in the metallization is negligible and that of the inductances is obviously nil). The device is working in the transistor-transistor current gain regime (Fig. 7a) which is responsible for the low conduction losses. The negative gate voltage on the gate terminal initiates the current commutation from the cathode to the gate. This process is slower for the GCT segments that lie farther from the gate contact (ring 2). Nevertheless it is completed (t_1 in Fig. 6a and Fig. 6b) before any significant voltage is supported across the main junction of the device (J2 shown in Fig. 4b) which is the first requirement for a successful turn-off. This is called the ‘Hard Drive’ requirement. At this point all the n+ emitters are isolated ($I_{K,1}$, $I_{K,2,1}$ and $I_{K,2,2} = 0$) and the anode voltage ramp phase follows. During the initial stages of this phase, the device operates as an open base p-n-p transistor (Fig. 7b). When the device already supports a voltage drop in excess of 2000V, the presence of high electric field with high conduction current induces carrier generation by dynamic avalanche. This reduces the rate of voltage rise (dV_A/dt), identified in the anode voltage waveform by the characteristic “knee” at the onset of change of the rate, time period t_2 - t_3 in Fig. 6a (and t_2 - t_3' in Fig. 6b).

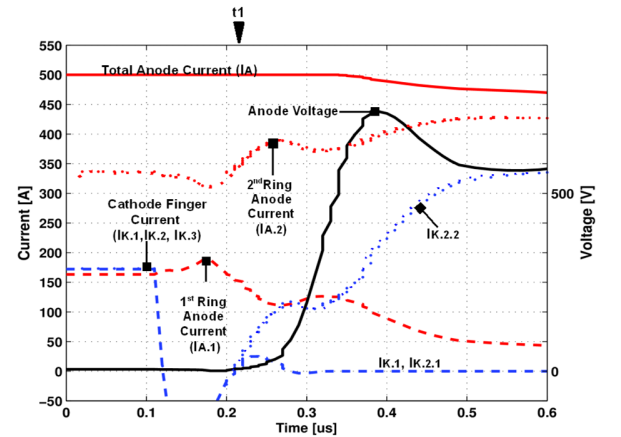
The dynamic avalanche current generation serves as the base current of the inherent p-n-p transistor of the device. This can be identified as an avalanche-transistor positive feedback current gain mechanism which is depicted in Fig. 7c. Throughout this phase there is a current shift from the region of the wafer that is closer to the gate contact to the farthest silicon area. This can be explained by the fact that this region has slower depletion propagation during the initial moments of the turn-off, thus it forms a more preferable path for the current. Indeed this current redistribution is accelerated and enhanced by the avalanche-transistor current gain mechanism. When the anode voltage reaches the DC-link voltage (VD), time instance t_3 in Fig. 6a, the current starts to redirect in the FWD, thus the conduction current starts to reduce. This is the beginning of the current fall phase.



(a) Successful turn-off simulation ($I_{on}=300A$, $V_D=2.7kV$)



(b) Catastrophic turn-off simulation ($I_{on} 360A$, $V_D=2.7kV$)



(c) Catastrophic turn-off simulation ($I_{on} 500A$, $V_D=500V$)

Fig. 6. Successful (a) and catastrophic (b, c) turn-off simulations (3D)

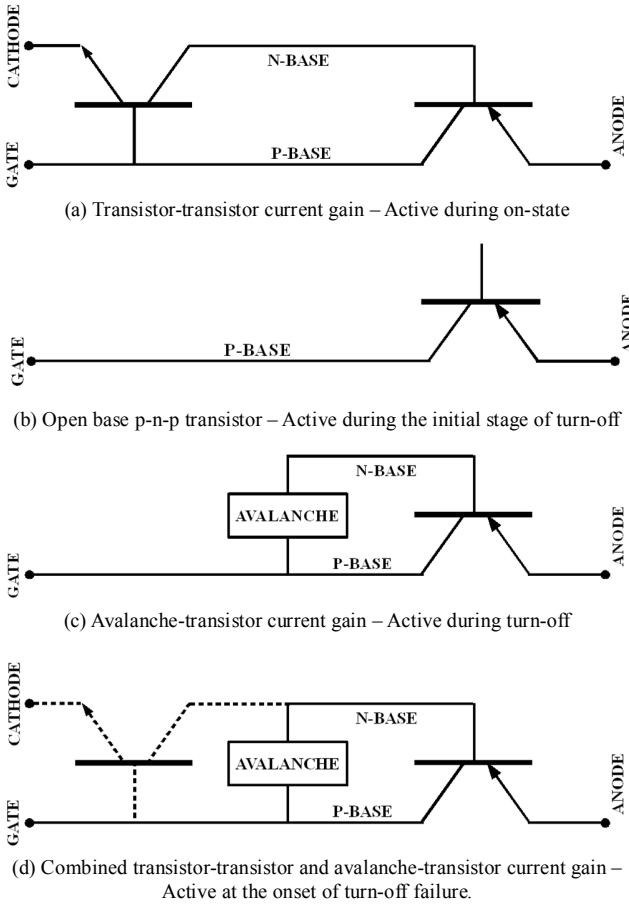


Fig. 7. Modes of operation and the current gain positive feedback mechanisms in GCTs

When the conduction current is increased to a value outside the controllable range of e.g. 340A at $V_D=2.7\text{kV}$, the device fails to turn off ($260\text{kW}/\text{cm}^2$). The waveform for the failure turn-off is depicted in Fig. 6b. The carrier ionization in the depletion region (which also serves as the base current of the p-n-p transistor) remains active until the end of the turn-off. This positive feedback current gain mechanism (Fig. 7c) is always more intense in the remotest regions of the wafer which leads to a localized increase in the current share. This is also in good agreement with measurements of failure phenomena in inductively loaded GTO thyristors in snubberless inductive switching [16]. At the onset of turn-off failure, the current flowing beneath one or more cathode segments (which also serves for the base current of the n-p-n transistor) becomes high enough to trigger the thyristor regenerative action (time instance t_3' in Fig. 6c). The combined transistor-transistor and avalanche-transistor positive feedback mechanism (Fig. 7d) creates a local highly conductive path (depicted in Fig. 8) which leads to the failure.

At low supply voltages e.g. $V_D=500\text{V}$, the device can safely turn off a load current (I_{on}) up to 480A. When the device current is increased (Fig. 6c), the device fails to turn off right at the beginning of the turn-off cycle. The mechanism behind this failure is however different from the one described above. The cathode/gate junction (J1 shown in Fig. 4b) of a

cell in the outermost ring fails to get reverse biased before the main junction, J2, starts supporting the voltage drop which violates the condition for hard-drive. This GTO turn-off mode cannot be tolerated in GCTs due to the absence of snubbers.

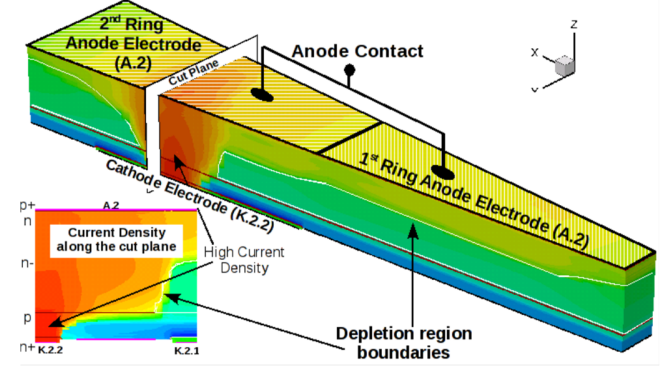


Fig. 8. The current density in the device (anode side up) at time instance t_3' in Fig. 6b. One of the outermost cathode segments (K.2.2) in the second ring re-triggers during the turn-off

The turn-off failure dependence on dynamic avalanche

In order to give the complete picture of the conditions that lead to the final destruction in Gate Commutated Thyristor devices and the role of the dynamic avalanche current, the 3D MCC simulations were repeated without the avalanche model enabled. Fig. 9 depicts the turn-off waveform with the avalanche model in the simulator deactivated. At $I_{on}=360\text{A}$ and $V_D=2.7\text{kV}$, the GCT can safely turn-off in contrary to the case where the avalanche phenomenon is taken into account. Important differences in the waveform of Fig. 9 when compared with Fig. 6b are: 1. the anode voltage rise does not suffer from a dV_A/dt change and 2. there is no current redistribution in the device.

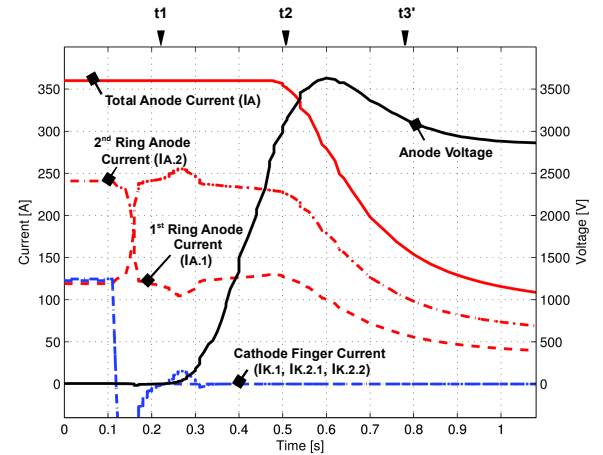


Fig. 9. Turn-off simulation waveform with the avalanche model deactivated for $I_{on}=360\text{A}$ and $V=2.7\text{kV}$

Fig. 10, Fig. 11 and Fig. 12 depict how the carrier concentration, the quasi-Fermi potential (Q_F) and the electron current density vary in the region of the device that fails with and without the avalanche model. They correspond to the time instances t_1 , t_2 and t_3' depicted in Fig. 9 and Fig 6 respectively.

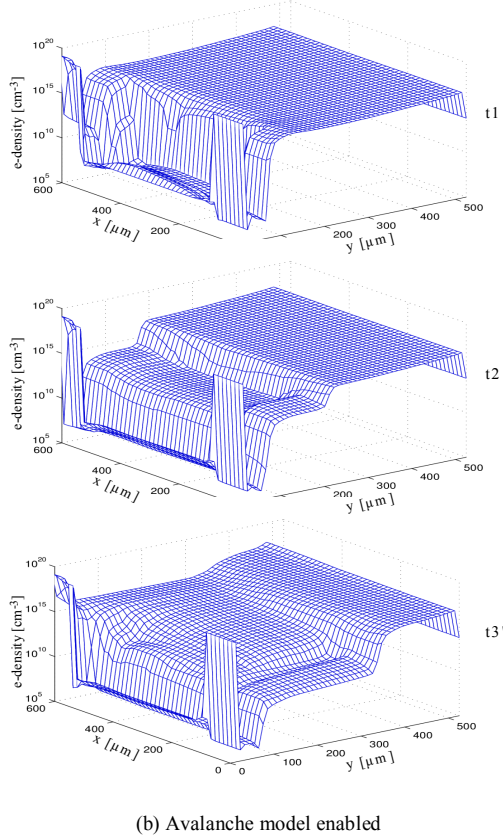
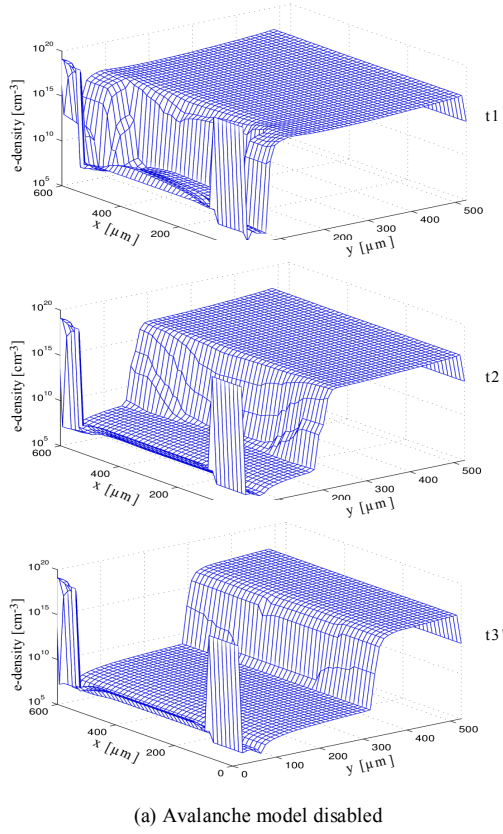


Fig. 10. Electron density during turn-off without and with the avalanche models enabled for the equivalent time instances t1, t2 and t3' in Fig. 9 and Fig. 6b along the cut plane shown in Fig. 8.

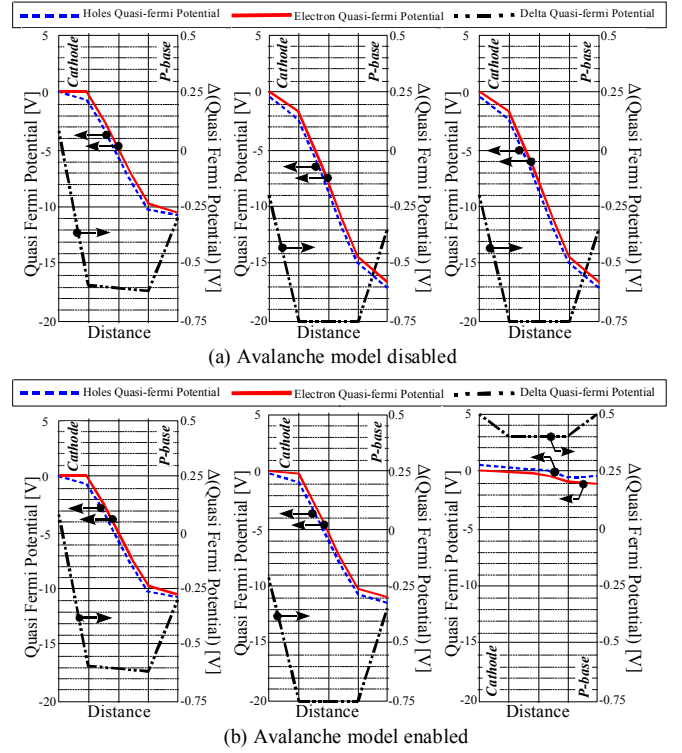


Fig. 11. The Quasi-Fermi potential band diagram along the middle of K2.2 cathode/p-base junction for the equivalent time instances t1, t2 and t3' in Fig. 6b and Fig. 9.

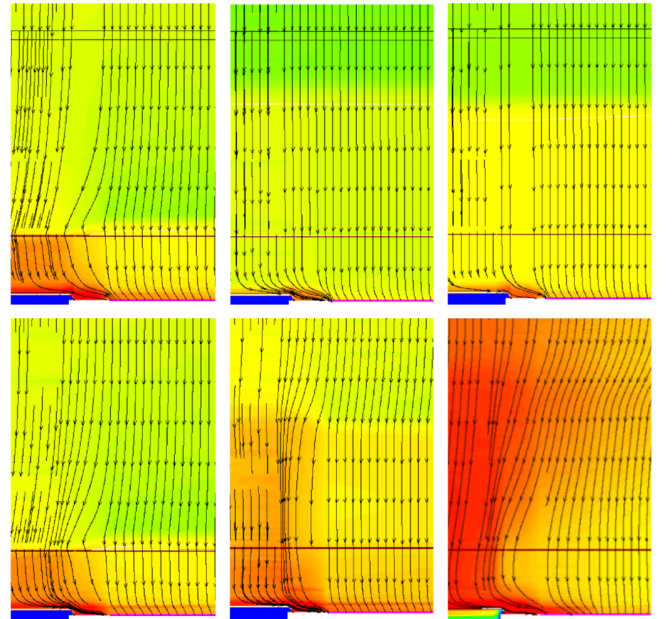


Fig. 12. The current density in the device during turn-off for without (top) and with (bottom) avalanche enabled for the equivalent time instances t1, t2 and t3' in Fig. 9 and Fig. 6b along the cut plane shown in Fig. 8.

During the initial stage of the turn-off (t1), the carrier maps are identical for the case where avalanche is enabled or not. This indicates that the avalanche does not affect the hard drive limit. The region beneath the cathode segments has the mobile charges depleted fast and the injection cuts off for both scenarios, with and without avalanche enabled. During the

next stage of the turn-off where the depletion of excess carriers progresses deeper into the p-base and the n-drift regions, the carrier maps start to differentiate. In particular the avalanche maintains the concentration of free carriers to a much higher level. The carrier density is larger beneath the cathodes which in turn causes the conduction current to focus in that proximity (Fig. 12). This increased lateral current density strongly increases the Quasi-Fermi potential difference in the middle of the cathode/p-base junction. At the onset of failure, the current flowing becomes large enough to locally compensate the potential barrier of this junction and to cause re-triggering of the thyristor. This floods the region nearby with plasma (Fig. 10) and the depletion collapses completely. This highly conductive region takes over the whole load current and leads to the final failure of the device.

A comparison of the MCC simulations with and without the avalanche model reveals the dominating failure mechanisms at various VD. The conclusive results are depicted in Fig. 13. The first failure mechanism dominates at low supply voltage (up to 2000V), the second mechanism is distinctive in the voltage range 2.2kV to 3.3kV. Indeed the device always fails by reaching the limits of the hard drive when the avalanche effects do not take place.

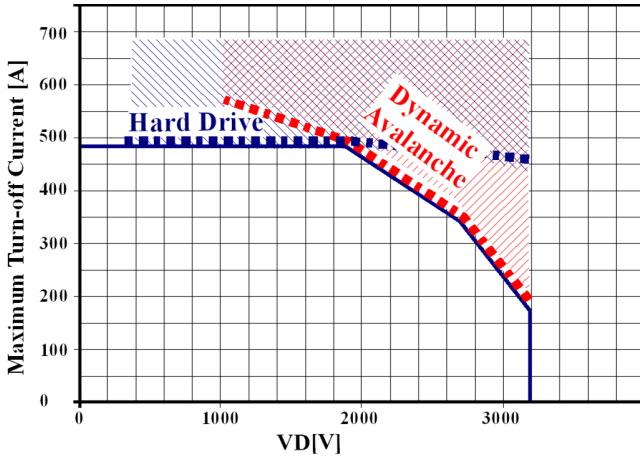


Fig. 13. Dominating Failure Mechanisms

Temperature dependence

The 3D model is ideal to investigate how the MCC spectrum is shaped by the temperature because it has already been verified with experimental results at 388K. The simulation procedure is identical with the one already described. The junction temperature is first set at a specific level, and then the MCC test is performed with a supply voltage varying from 500V to 3000V. The results are summarized in Fig. 14.

At low DC link voltage (up to 1.9kV), the failure mechanism is dominated by the violation of the conditions for hard drive operation i.e. the cathode/p-base region is not completely depleted to bring the GCT in the p-n-p transistor mode prior a significant voltage drop in the device. In this supply voltage range, the Maximum Controllable Current increases with reducing temperature. The increase in the MCC when the temperature is reduced from the 388K to 300K is

proportional to the reduction in the temperature. This is due to the proportional increase in the cathode/p-base junction voltage (with a slope of ~ -1.8 mV/K). Hence, an increased conduction current is required for the built-in junction voltage to be overcome. At the increased temperature of 413K the plasma concentration in this region grows which makes the establishment of the cathode/p-base depletion more difficult, the bipolar gain increases in addition to the reduction in the junction voltage. Hence at 413K the reduction in the MCC is disproportional to the ratio of increase of temperature.

At high supply voltage values $VD=1900V$ to $VD=3100V$, the dominating failure mechanism is avalanche driven. The MCC reduces with increasing temperature from 388K to 413K because of the same reasons discussed above but also due to the extra carriers' generation by dynamic avalanche. Interestingly the MCC reduces even further when the temperature is reduced from 388K to 300K. This is in opposition to the observed trend in the supply voltage range up to $VD=1900V$. This is justified by the increase in the avalanche coefficients. By reducing the temperature, the avalanche coefficients increase according to the formula [17]:

$$\alpha(E) = \left(\frac{qE}{E_i} \right) \exp - \frac{E_i}{E \left[1 + \frac{E}{E_p} \right] + E_T},$$

where α is the ionization coefficient, E is the electric field and E_p , E_T and E_i are the electric field at which the carriers overcome the decelerating effects of phonon, temperature and ionization scattering respectively. At 300K the ionization of charge by dynamic avalanche increases to such an extent that dominates the MCC trend and overcomes the results of the increasing junction voltage. At the normal operating DC link voltage, $VD=2.7kV$, the maximum controllable current is achieved at $T_J=388K$.

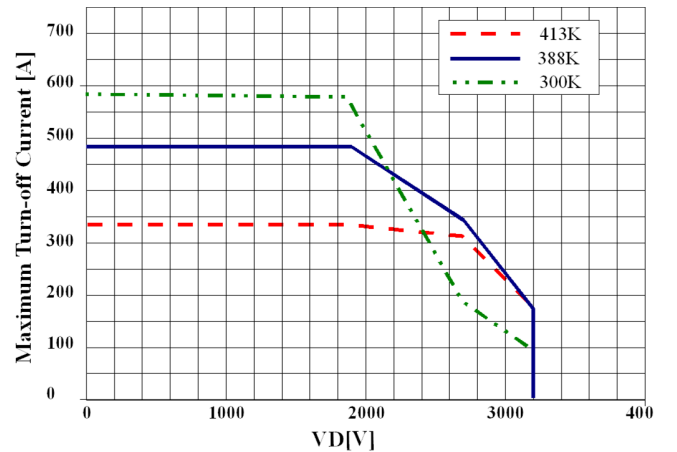


Fig. 14. The temperature dependence of the Maximum Controllable Current at different DC link voltages.

IV. CONCLUSIONS

The full wafer geometrical structure and the parasitics of GCT devices strongly reflect on the device behavior in dynamic conditions. An accurate three dimensional wafer level

simulation tool which takes into consideration the geometrical lack of homogeneity can analyze a large area GCT giving very good matching with experimental data. The 3D FEM structure incorporated in a mix-mode simulator together with the SPICE components of a realistic test circuit gives a deep physical insight of the device dynamics. In this paper we provide a complete analysis of the turn-off of a 24mm in diameter GCT. In particular the dominating mechanisms are identified over a range of supply voltages. We also identify the temperature and avalanche dependence of the Maximum Controllable Current. Indeed the dynamic avalanche controls the Maximum Controllable Current and an optimized device structure can report high MCC only alongside a greater ability to resist the adverse effects of dynamic avalanche. In the limit of maximum MCC a device should decouple completely the avalanche current from the failure mechanism. The model used in this paper can also be used to analyze the turn-off performance and the tolerance in dynamic avalanche of different GCT structures including the High Power Technology (HPT) or novel GCTs which feature corrugated p-base.

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