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Experimentally Validated Three Dimensional GCT Wafer Level Simulations

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Abstract— **In this paper we present a wafer level three-dimensional simulation model of the Gate Commutated Thyristor (GCT) under inductive switching conditions. The simulations are validated by extensive experimental measurements. To the authors' knowledge such a complex simulation domain has not been used so far. This method allows the in depth study of large area devices such as GCTs, Gate Turn Off Thyristors (GTOs) and Phase Control Thyristors (PCTs). The model captures complex phenomena, such as current filamentation including subsequent failure, which allow us to predict the Maximum Controllable turn-off Current (MCC) and the Safe Operating Area (SOA) previously impossible using 2D distributed models.**

I. INTRODUCTION

Latching devices consist of a four-layer pnpn structure and have the most competitive on-state performance and blocking characteristics in the very high power range of the power semiconductor device spectrum. Nevertheless turning off those devices has always been a challenge. The introduction of the GCT [1] aimed to alleviate the problems encountered during turn-off by switching off the device in transistor rather than in thyristor mode. Through application specific performance tailoring and design improvements of the device and the driving circuit, the GCT gained a large market share in high power applications such as Medium Voltage Drives (MVDs), inverters, power quality control and traction. However scalability problems, related to large area structures (such as full wafers) still exist [2, 3, 4, 5].

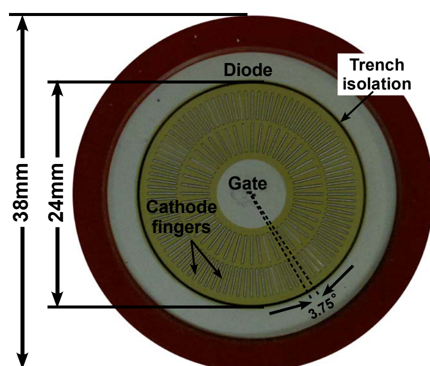


Fig. 1: 38mm Reverse-Conducting IGCT wafer

The turn-off process in GCTs is difficult to study because of its three dimensional nature. The interaction between neighboring cells is important and an accurate model has to take all the geometrical features of such a composite device into account. A wafer level 3D model is therefore of utmost importance. A 3D semiconductor model for such a device has been long awaited from the semiconductor community, but only recently computational methods have made this possible [6].

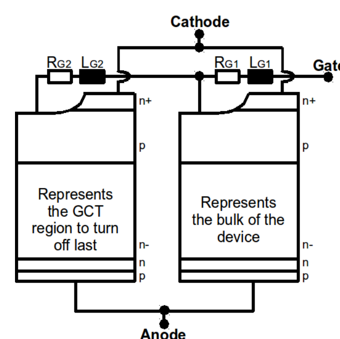


Fig. 2: Traditional 2D model with parasitic gate resistance (R_{G1}, R_{G2}) and inductance (L_{G1}, L_{G2}) for wafer simulations
R_{G1}=0.65mΩ, L_{G1}=0.4nH, R_{G2}=0.88mΩ, L_{G2}=0.6nH

The traditional representation of the GCT wafer used for simulations is two-dimensional and it is diagrammatically shown in Fig. 2. This model of parallel connected cells [3, 7] assumes symmetry with fixed cathode-gate interdigitation. It consists of two numerical unit GCT cells with individual cathode, anode and gate electrodes. One cell represents the region in the device that turns off last whereas the other one represents the bulk of the device. The respective cell electrodes are connected together via a SPICE circuit which makes up for the electrical coupling in the wafer. Thermal interaction, current and space charge traveling from one cell to the other via silicon are thus ignored. This model however accounts for the parasitic inductance and resistance due to the gate metalization. These parasitics are modeled by a network of resistances and inductances which introduce uneven delays in the turn-off signal between two distinctive regions in the GCT wafer device, the one closer to the gate contact and the one farther from it. These unit cells are identical in doping profile and scaled up in the "third" dimension to make up for the approximate area of the equivalent wafer region that they represent.

II. METHOD

In this work we used a 4.5kV reverse-conducting IGCT with a 38mm diameter. The GCT part of this device (in Fig. 1)

has a 24mm diameter and an active area of 3.5cm^2. It consists of long and narrow cathode fingers surrounded by the gate metallization which makes the gate contact terminal in the middle of the wafer. These fingers are positioned in two concentric rings and are connected together by a molybdenum contact disk held in place by the press-pack packaging.

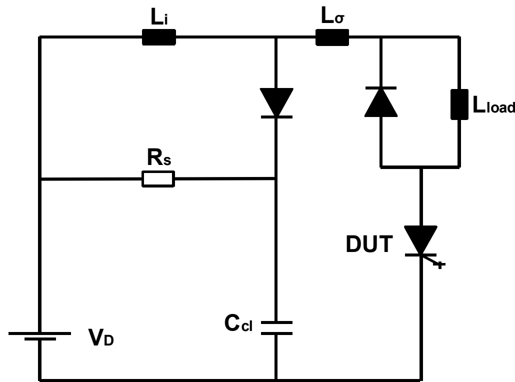
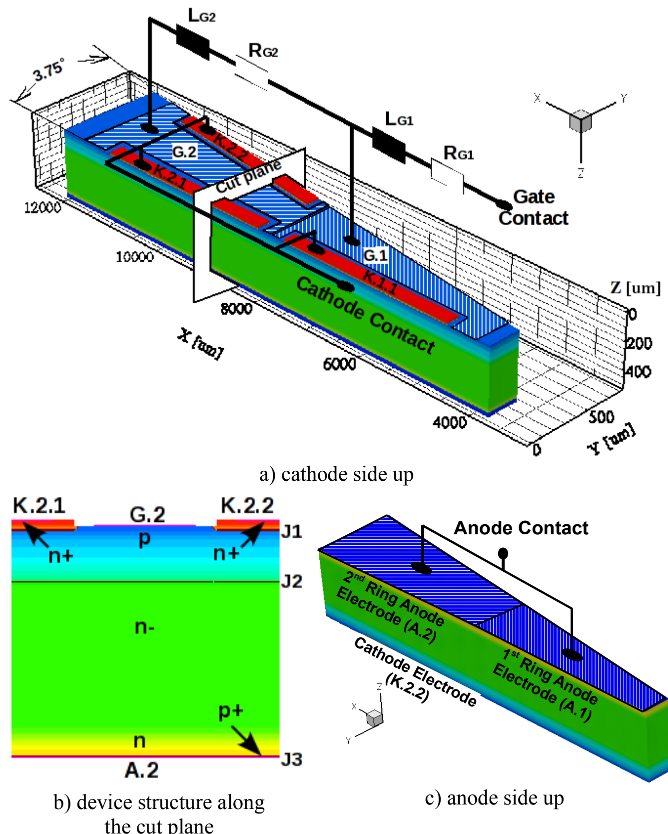


Fig. 3: The external circuit as used in the simulations
di/dt Limiting Inductor Li=25µH, Clamp Capacitor Ccl=0.5µF, Stray Inductance Lσ=1µH, Damping Resistor R_S=4.2Ω

The device was tested as when used in standard applications i.e. inverter circuits or choppers. The test circuit used throughout this paper is shown in Fig. 3. It has a di/dt and over-voltage clamp but no dV/dt snubbers. The extracted on-state characteristics at a junction temperature (T_J) of 115°C are shown in Fig. 5 and the snubberless SOA is shown in Fig. 6.



a) cathode side up

b) device structure along the cut plane

c) anode side up

Fig. 4: An angular slice of 3.75° of the 3D simulation domain with parasitic gate resistance (R_{G1}=0.65mΩ, R_{G2}=0.85mΩ) and inductance (L_{G1}=0.4nH, L_{G2}=0.6nH)

Fig. 4 shows the 3D model which is identical in 3D dimensions and physical profile to the GCT region of the 38mm Reverse-Conducting GCT shown in Fig. 1. The device dimensions for this GCT are at least three orders of magnitude larger than those in conventional 3D MOSFET or IGBT cells which makes it very demanding in computational power. Furthermore, it is challenging to transfer the wafer geometrical complications into a valid 3D numerical structure with an optimized mesh number of points.

The simulation domain used in this 3D model addresses the problem of absence of symmetry in the third dimension. As shown in Fig. 4, the gate electrode is split into two concentric regions, each one surrounding the cathode fingers of the equivalent concentric ring. This split-gate arrangement allows to introduce a network of SPICE resistances and inductances which make up for the varying inductance-resistance experienced on the gate region of the wafer device. Similarly the anode electrode on the bottom side of the angular slide is also split into two regions. These two regions are however connected to the same SPICE node making up the Anode Contact. By having two individual electrodes, one to cover the anode area of the inner ring and another one to cover the outermost anode ring region, the model gives a quick way to get readings of the anode current in the first and second ring without having to extract it from the numerical device. The cathode fingers are also shorted together on one SPICE node which makes up for the cathode contact of the GCT.

Both device models were tested using a SPICE representation of the circuit shown in Fig. 3. Initially they were matched against the experimental on state characteristics and then the SOA test was performed. The determination of the maximum turn-off current (IITGQ) requires a large number of mixed-mode simulations as one simulation can only predict whether the device was able to switch off safely or not. For every DC link voltage (V_D) the junction temperature is fixed to 115°C, the circuit components are kept constant and the device models turn off a certain current. Every successful turn-off is followed by another turn-off simulation of increased current until a SOA failure is recorded.

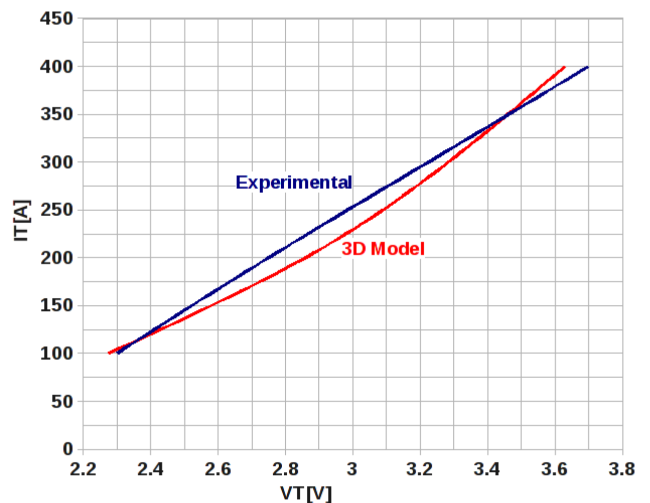


Fig. 5: On State Matching between the 3D model and measurements at T_J=115°C (VT and the IT are the on state voltage and current respectively)

III. SOA PREDICTION AND FAILURE MECHANISMS

Fig. 5 shows the simulated on state characteristics of the 3D GCT model overlaid on experimental measurements. Fig. 6 shows a comparison between the two simulation models on their capability to predict the Safe Operating Area overlaid on the experimental observations. As shown, the 3D model is able to switch off a current close to the experimental whereas the 2D model gives an overestimated SOA result.

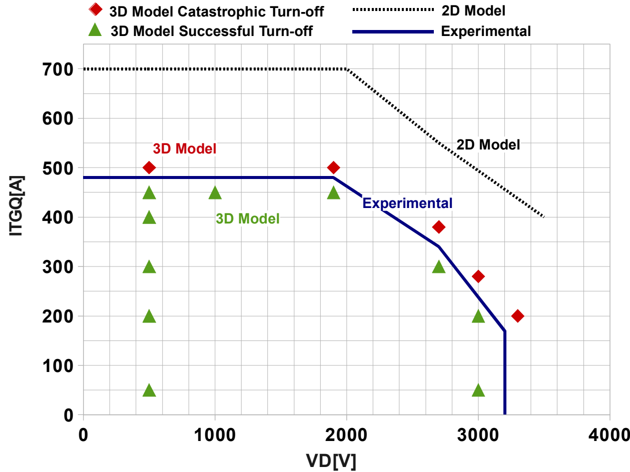
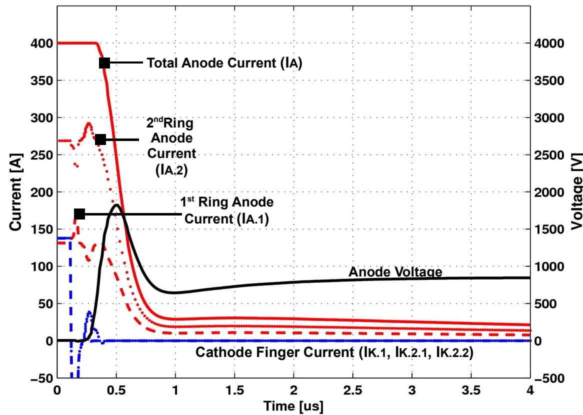
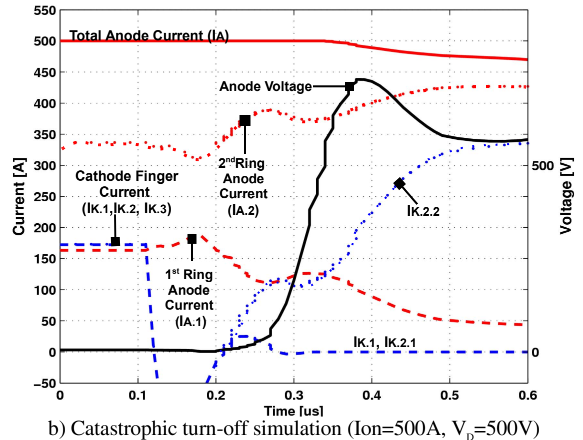


Fig. 6: The turn-off current capability ITGQ at supply voltage V_D



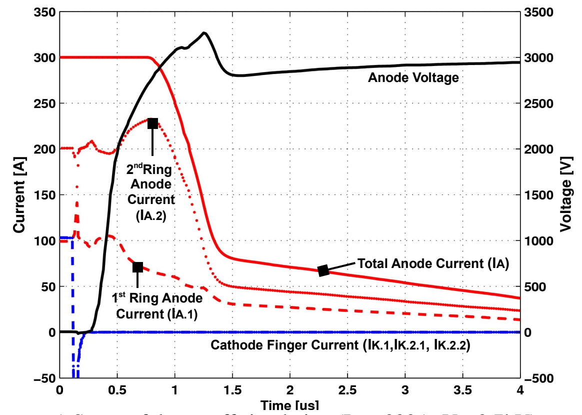
a) Successful turn-off simulation (Ion=400A, V_D=500V)



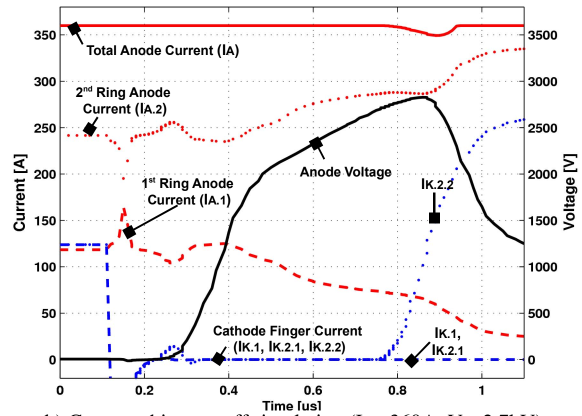
b) Catastrophic turn-off simulation (Ion=500A, V_D=500V)

Fig. 7: Successful (a) and catastrophic (b) turn-off simulation (3D) at low voltage, high current

The 3D simulations revealed two distinctive failure mechanisms. The first one dominates at low supply voltage (up to 2000V) and it is shown in Fig. 7. At a supply voltage V_D of 500V the device can safely turn off a load current Ion up to 480A. The cathodes stop emitting ($I_{K.1}$, $I_{K.2.1}$ and $I_{K.2.2}$ =0) and get reverse biased before a considerable voltage starts to be supported in the main junction (J2 shown in Fig. 4b) of the device. The anode current remains unaffected until the device anode voltage reaches the supply voltage V_D. Thereafter the anode current falls. A successful turn-off waveform is shown in Fig. 7a. When the device current is increased (Fig. 7b), the device fails to turn off right at the beginning of the turn-off cycle. The cathode/gate junction (J1 shown in Fig. 4b) of a cell in the outermost ring fails to get reverse biased before the main junction starts supporting voltage which violates the condition for hard-drive. This GTO turn-off mode cannot be tolerated in GCTs due to the absence of snubbers.



a) Successful turn-off simulation (Ion=300A, V_D=2.7kV)



b) Catastrophic turn-off simulation (Ion 360A, V_D=2.7kV)

Fig. 8: Successful (a) and catastrophic (b) turn-off simulation (3D) at high voltage, high current.

The second mechanism is distinctive in the voltage range 2.2kV to 3.3kV. As shown in Fig. 8, the imbalances and the geometry cause a current shift from the core of the wafer to the periphery of the wafer. During the voltage increase, the depletion region expands, the effective bases decrease and both the current gain of the pnp and the npn transistor (α_{pnp} and α_{npn} respectively) increase steadily. The dynamic avalanche becomes important when the anode voltage is greater than 2000V because of the coexistence of high electric field and conduction current. The avalanche current is multiplied by the

transistor gain which maintains the conduction current high in the outermost ring. The increasing current density in the proximity of the outermost ring introduces a disproportionally larger ionization effect making this region first to meet the requirement for re-triggering: the current flowing through the space charge region of the blocking junction (see Fig. 9 at the point of cross section) becomes large enough to locally compensate the potential barrier of this junction and to cause re-triggering.

Fig. 9 depicts the current density in the simulated device sector right after re-triggering. The high injection of electron current turns on the device locally and the depletion region collapses. This localized high power dissipation is what causes the wafer to burst in the destructive experiments.

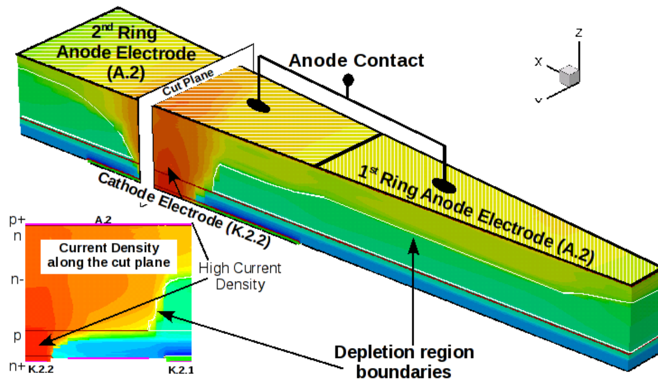


Fig. 9: The current density in the device (anode side up). One of the outermost cathode fingers (K2.2) in the second ring re-triggers during the turn-off.

IV. DISCUSSION

The new 3D GCT model demonstrates both qualitative and quantitative agreement with the experimental results. The comparison of simulated and measured SOA on Fig. 6 confirms a very good predictive capability of our simulations. The traditional 2D parallel cell model is able to analyze the on-state phenomena, but fails to capture failure modes during turn-off and therefore unable to predict the maximum current controllability and the underlying destruction mechanisms. Compared to the 2D, it is the true 3D device simulation which allows us to take into account all relevant non-uniformities and parasitics, which drive the device into the turn-off failure.

Advantages of this 3D model:

- Interaction between different areas inside the device is taken into account, especially in the proximity of the parallel operating cathodes.
- The geometrical and physical features of the wafer are considered.
- It can capture the turn-off process and hence predict the MCC and SOA in large area devices like GCTs and GTOs.
- Significantly decreases the number of steps in the device design and optimization, hence substantially reducing the design cycle. Less designs need to be fabricated and verified.
- Provides deep physical insight into complex phenomena such as current filamentation and dynamic avalanche.

V. CONCLUSION

An accurate wafer level simulation tool can analyze a large area GCT with the real application circuit giving very good matching with experimental data. Such a model can predict with high precision the SOA. The dynamics of such a SOA failure can also be analyzed. This is important especially for the bipolar sector, which is constantly moving to larger dimensions where geometry, and in particular the 3D nature of it, strongly affects the operation of the device [8].

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