

# Novel Approach Toward Plasma Enhancement in Trench-Insulated Gate Bipolar Transistors

Antoniou, M, Lophitis, N, Bauer, F, Nistor, I, Bellini, M, Rahimo, M, Amaratunga, G & Udrea, F

**Author post-print (accepted) deposited by Coventry University's Repository**

**Original citation & hyperlink:**

Antoniou, M, Lophitis, N, Bauer, F, Nistor, I, Bellini, M, Rahimo, M, Amaratunga, G & Udrea, F 2015, 'Novel Approach Toward Plasma Enhancement in Trench-Insulated Gate Bipolar Transistors' *Electron Device Letters*, vol 36, no. 8, pp. 823-825  
<https://dx.doi.org/10.1109/LED.2015.2433894>

DOI 10.1109/LED.2015.2433894

ISSN 0741-3106

ESSN 1558-0563

Publisher: IEEE

**© 2015 IEEE. Personal use of this material is permitted. Permission from IEEE must be obtained for all other uses, in any current or future media, including reprinting/republishing this material for advertising or promotional purposes, creating new collective works, for resale or redistribution to servers or lists, or reuse of any copyrighted component of this work in other works.**

Copyright © and Moral Rights are retained by the author(s) and/ or other copyright owners. A copy can be downloaded for personal non-commercial research or study, without prior permission or charge. This item cannot be reproduced or quoted extensively from without first obtaining permission in writing from the copyright holder(s). The content must not be changed in any way or sold commercially in any format or medium without the formal permission of the copyright holders.

This document is the author's post-print version, incorporating any revisions agreed during the peer-review process. Some differences between the published version and this version may remain and you are advised to consult the published version if you wish to cite from it.

# Novel approach towards plasma enhancement in Trench Insulated Gate Bipolar Transistors

M. Antoniou, N. Lophitis, F. Bauer, I. Nistor, M. Bellini, M. Rahimo and F. Udrea

**Abstract**— In this paper a Trench IGBT design with “local” charge compensating layers featured at the cathode of the device is presented and analysed. The Superjunction or Reduced Surface (RESURF) effect proves to be very effective in overcoming the inherited on-state versus breakdown tradeoff appearing in conventional devices such as the Soft Punch Through Plus (SPT+) or Field Stop Plus (FS+) IGBTs. This design enhances the on-state performance of the FS+ IGBT by increasing the plasma concentration at the cathode side without affecting either the switching performance or the breakdown rating.

**Index Terms**— Insulated Gate Bipolar Transistor (IGBT), superjunction power MOSFET, technology trade-off.

## I. INTRODUCTION

THE IGBT structure has been through a remarkable evolutionary path since its invention with all subsequent steps focusing primarily on enhancing the device static and switching performance. Starting from the DMOS gate configuration, the introduction of the trench gate enhanced the PiN diode effect (electron injection) at the cathode side of the device. Moreover, the Soft Punch Through and the Field Stop wafer technologies for the DMOS and Trench IGBTs respectively resulted in a dramatic decrease in the on-state and switching losses due to the wafer thinning and anode injection control. The next major improvement came for the addition of “n enhancement” layer with the aim of further increasing the electron injection at the cathode side of the drift region. Some of the most effective designs in achieving this include the IEGT (Injection Enhanced Gate Transistor)[1,2], the CSTBT (Carrier Store Trench Bipolar Transistor)[3], the Trench EST (Emitter Switched Thyristor)[4,5], the HiGT (High Conductivity IGBT) [6,7] and the DMOS SPT+ IGBT (Soft Punch Through plus)[8]. The higher the doping concentration of the “n enhancement”, the more significant the improvement in the on-state characteristics is. However, the doping concentration of the n enhancement layer cannot be increased

Manuscript received May 4, 2015; accepted May 9, 2015. Date of publication May 15, 2015. The review of this letter was arranged by Editor S.-H. Ryu.

M. Antoniou, N. Lophitis and F. Udrea are with the Department of Electrical Engineering, University of Cambridge, Cambridge CB2 1TN, U.K. (e-mail: ma308@cam.ac.uk).

F. Bauer, I. Nistor, and M. Bellini are with ABB Switzerland Ltd., Corporate Research, Baden-Datwil 5405, Switzerland.

M. Rahimo is with ABB Switzerland Ltd., Semiconductors, Lenzburg 5600, Switzerland.

Color versions of one or more of the figures in this letter are available online at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/LED.2015.2433

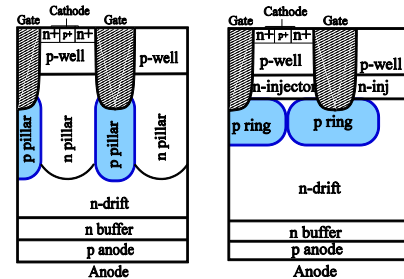


Fig.1. (a) The semi-SJ IGBT structure and (b) Compensating p-ring structure (not to scale).

interminably because it strongly affects the blocking capability. In this work a novel design has been employed which allows to further improve the state-of-the-art technology curve of IGBTs by compensating the n-enhancement layer charge with that of a p-doped layers. It allows the increase in the doping concentration of the n-enhancement layer without compromising the blocking capability similarly to what is done in SuperJunction devices such as Cool MOS [9]. As a result, the implementation of the proposed structure leads to a major reduction in the on-state losses. The proposed structure has been evaluated against its conventional counterpart which will be referred as the Trench FS+ IGBT.

## II. DEVICE STRUCTURE

Previously the authors have reported on the advantages of the utilization of the SuperJunction technology in the IGBT structure [10] where the drift region is composed of alternating p and n-layers extending towards the anode of the device. In the semi-SJ IGBT structure depicted in Fig. 1(a) [11], the p-pillars are not connected to the p-base so the conductivity modulation at the cathode side of the drift region is not affected. Nevertheless, due to the presence of the superjunction the electric field distribution of the semi-SJ IGBT is flat across the top drift region and it is this property that helps the device to withstand higher voltages before breaking as well as significantly increase the device cosmic radiation resilience.

A direct application of this concept is presented in this paper; the “p-ring Trench FS+ IGBT” is depicted in Fig. 1(b). The anode side of this IGBT structure features an n-buffer and p-anode layer. The cathode side employs a trench gated structure, an n doped enhancement (n injector) and p doped buried layers (p-rings). In this structure the level of the n-injector doping was increased so that to allow a further reduction in the on-state losses when compared to the state-of-the-art. In the conventional FS+ IGBT design, the n-

enhancement layer doping is  $7 \times 10^{16} \text{cm}^{-3}$ . In this work the n-enhancement layer doping concentration was lifted by almost one order of magnitude while the doping concentration of the p-rings was adjusted accordingly; the p-ring charge compensates part of the increased n layer doping charge similarly to the SuperJunction. Fig.2 shows the doping concentration (a.u) of the various cathode side layers along the cutline at the cathode side of the device. An additional advantage of the proposed design is the ease of manufacturability and the compatibility with the standard process flow; the demonstrated device does not require extra masks because the p-rings can be formed by implanting Boron through the trench opening immediately after etching it. A similar p-ring implantation through the trench is reported in [12], but no n-enhancement layer is present. A Scanning Electron Microscope (SEM) picture of the fabricated “p-ring” Trench FS+IGBT is shown in Fig. 3. As shown, the compensating p-rings were formed under the trenches as predicted through the process simulation (Fig. 2). The n-injector layer is not contained within the p ring layer as it connects to the n-drift on the one side of the trench but not the other (Fig. 1a, 2 and 3). The effect achieved is similar to that reported in [13], with the main difference here being the introduction of the p-rings through the gate trenches. In [13] thyristor action is shown (via simulations) through the p ring, but this relies on electron injection from an accumulation layer rather than from the n enhancement. Cluster IGBT [14] also displays a thyristor action with enhanced electron injection. In the CIGBT the p-well encloses the n-well and isolates it from the drift region; this is not the case in our structure and no charge compensation between the n-well and p-well is discussed in [15]. The charge compensation between the p-ring and the n-enhancement is essential here for achieving a superjunction effect.

Under this experimental setup the mesa width achieved is  $0.8 \mu\text{m}$  which advances the state-of-the-art dimensions (fig.4). It is worth noting that the source contact within the mesa regions has its minimum possible lateral extension and clearance from the trenches walls ( $0.4$  and  $0.2 \mu\text{m}$  respectively). A very narrow spacing between conducting trench channels allows for a significant reduction in on-state losses. The underlying principle is that the narrower pitch impedes the hole collection while increasing locally the electron current density as explained in detail below. This results in higher local electron injection and hence better conductivity modulation of the drift region. This phenomenon has been the subject of research in [15, 16] and is also referred to as ‘point injection [17]. Preliminary results of this work appeared in [18].

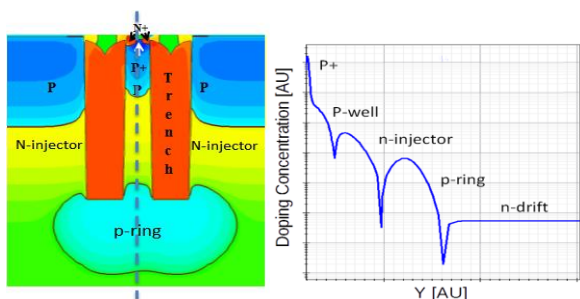


Fig. 2. The simulated compensating p-ring structure.

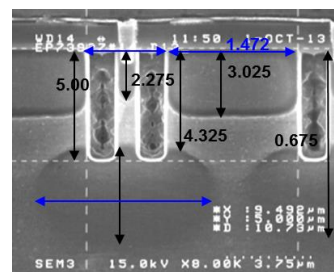


Fig. 3. SEM picture of the fabricated “p-ring” Trench FS+IGBT.

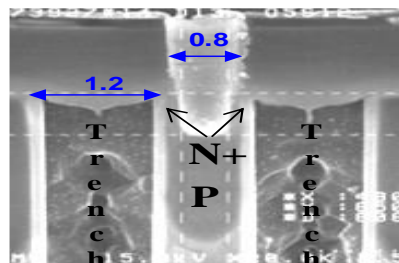


Fig. 4. The mesa region of the “p-ring” Trench FS+IGBT .

### III. DEVICE OPERATION AND PERFORMANCE

#### A. Blocking state

The doping of the n-enhancement layer in a conventional structure is carefully chosen so that it is completely depleted and the breakdown is only marginally deteriorated by its presence. However to reduce further the on-state losses, the n-enhancement needs to have a significantly higher doping concentration. In this case, without the presence of the p-rings, the breakdown ability will be severely degraded. The p-ring is always electrically connected to the p-well both under blocking and on-state conditions. Under on-state conditions the gate bias keeps the p-ring connected to the p-well due to the formation of the inversion layer at the Si/Oxide surface. Under blocking conditions the n enhancement layer is completely depleted and as a result the p well is again connected to the p-ring. The p-ring and the resulting p-n blocks create a RESURF region in the vicinity of the cathode which in turn helps towards lowering the electric field in the proximity of the n-enhancement layer. As a result, the peak electric field is reduced and the blocking rating is maintained (in spite of the significant increase in the doping of the n-enhancement layer). Fig.5 shows the simulated electric field distribution across the cathode side of the device (n-inj doping at  $5 \times 10^{17} \text{cm}^{-3}$ ) with and without the p-rings. From this figure we can clearly see that the electric field peak is significantly

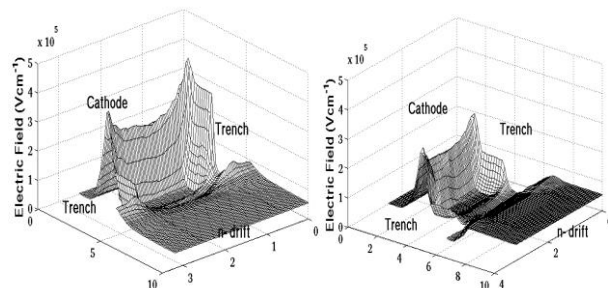


Fig. 5. Cathode side electric field distribution across the FS+ IGBT and p-ring FS+ IGBT at  $V_{\text{anode}}$  240 and 1.7kV respectively.

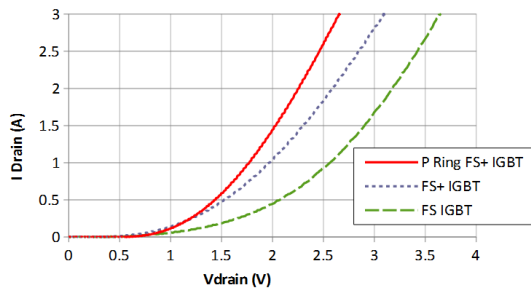


Fig. 6. On-state characteristic for the fabricated devices at 125°C.

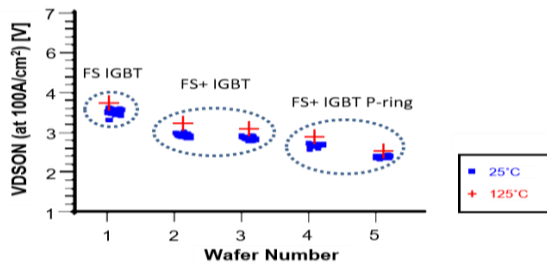


Fig. 7. On-state voltage for the fabricated devices at 25 & 125°C.

suppressed in the second case. Therefore, using this technique, the doping concentration of the n enhancement layer can be almost an order of magnitude higher compared to a conventional one, without compromising the breakdown rating of the device. For the RESURF to be effective however, the p-rings need to be carefully designed in order to correctly balance the increased in n-injector doping charge. Therefore, using this technique, the doping concentration of the n enhancement layer can be almost an order of magnitude higher compared to a conventional one, without compromising the breakdown rating of the device.

### B. On state

The electron current has a direct path to the drift region via the n-injector layer from the cathode contact, along the trench, into the accumulation layer of the p ring. Once the thyristor structure turns on, the p-ring is modulated similarly to [13]. Due to the fact that the PiN diode is active from the very beginning, no snapback phenomenon is observed during turn on. It is also worth noting that the PiN diode effect is the same as a thyristor effect from an on-state carrier conductivity modulation point of view [4].

Fig. 6 shows the fabricated structures on-state voltage characteristic at 125°C. The standard Trench IGBT and the Trench FS+IGBT have on-state voltage drops at 100A/cm<sup>2</sup> (3A) of around 3.6 and 3.1V. The “p-ring” FS+IGBT measured on-state voltage was around 2.6V, a decrease in on-state voltage drop of about 20%. The same percentage improvement is also achieved at 25°C as shown in Fig. 7. It is also important to note that the spread in the measurements is very small; this in turn is an indication of good reproducibility of the new “p-ring” FS+IGBT.

### C. Switching conditions

The enhanced performance of the device in the on-state is the result of additional plasma at the cathode side. The impact of high plasma concentration in the vicinity of the cathode is very small when compared to achieving an equivalent

improvement in the on state by engineering the plasma at the anode side. This is because this additional charge introduced is located very close to the main blocking junction of the device which is therefore very quickly removed during the initial stages of switching off. As a consequence, the proposed design has minimum effect on the switching losses.

## IV. CONCLUSION

In this paper a novel device design that enhances the Trench FS+IGBT performance, the p-ring structure, has been fabricated and tested. The “p-ring” layer under to the gate trench compensates for the increase in the n injector doping through a local RESURF effect. The presence of a highly doped n-injector layer results in significant on-state losses reduction without compromising the switching performance or the breakdown rating of the device and requires no additional mask for its realization. Therefore for the same switching losses the device can achieve up to 20% reduction of the on state energy losses compared to the FS+ IGBT at both 25 and 125°C.

## REFERENCES

- [1] M. Kitagawa et al. "A 4500 V injection enhanced insulated gate bipolar transistor (IEGT) operating in a mode similar to a thyristor", IEDM '93, pp.679-682.
- [2] T. Inoue et al., "New collector design concept for 4.5 kV injection enhanced gate transistor (IEGT)," ISPSD 2002, pp. 49- 52.
- [3] H. Takahashi et al. "Carrier Stored Trench-Gate Bipolar Transistors (CSTBT) - A Novel Power Device for High Voltage Application", ISPSD 1996.
- [4] P. Gough, "MOS-Gated Thyristor" US Patent No. 5202750, April 1993.
- [5] M.S Shekar et al; "Trench gate emitter switched thyristors", in Proc. 6th ISPSD, 1994, pp.189-194.
- [6] M. Mori et al. "A Novel High-Conductivity IGBT (HiGT) with Short Circuit Capability", ISPSD 1998.
- [7] K. Oyama et al. "Novel 600-V trench high-conductivity IGBT (Trench HiGT) with short-circuit capability," ISPSD 2001, pp.417-420.
- [8] M. Rahimo et al. "Novel soft-punch-through (SPT) 1700V IGBT sets benchmark on technology curve", Proc. PCIM, pp.393 -397 2001.
- [9] T. Fujihira "Theory of Semiconductor Superjunction Devices" 1997 Jpn J. Appl. Phys. 36 6254.
- [10] M. Antoniou et al., "The Soft Punchthrough + Superjunction Insulated Gate Bipolar Transistor: A High Speed Structure With Enhanced Electron Injection," IEEE Transactions on Electron Devices, vol.58, no.3, pp.769-775, March 2011
- [11] M. Antoniou et al., "The 3.3kV Semi-SuperJunction IGBT for increased cosmic ray induced breakdown immunity," In 21st International Symposium on Power Semiconductor Devices & IC's, ISPSD 2009, pp.168-171.
- [12] R. Constapel, et al. "Trench-IGBTs with integrated diverter structures," in Proc. 7th ISPSD, 1995, pp.201-206.
- [13] G. Amaratunga and F. Udrea "Semiconductor device having an insulated gate field effect transistor and exhibiting thyristor action" US Patent No. 5489787 Feb 1996.
- [14] O. Spulber et al. "A novel, 1.2 kV trench clustered IGBT with ultra high performance, ISPSD 2001, pp.323-326, 2001.
- [15] F. Udrea, "Novel MOS-gated bipolar device concepts towards a new generation of power semiconductor devices," Ph.D. Dissertation, Engineering Department, Univ. Cambridge, Cambridge, U.K., 1995.
- [16] A. Nakagawa, "Theoretical Investigation of Silicon Limit Characteristics of IGBT," ISPSD 2006, pp.1-4.
- [17] M. Antoniou et al, "Point injection in trench insulated gate bipolar transistor for ultra low losses" ISPSD 2012, pp.21-24.
- [18] M. Antoniou et al, "Experimental demonstration of the p-ring FS+ Trench IGBT concept: A new design for minimizing the conduction losses", ISPSD 2015, pp.1-4.