Retrograde p-well for 10kV-class SiC IGBTs

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Amit K. Tiwari, Marina Antoniou, Neophytos Lophitis, Samuel Perkins, Tatjana Trajkovic, and Florin Udrea

***Abstract*—In this paper, we propose the use of a retrograde doping profile for the p-well for ultra-high voltage (>10kV) SiC IGBTs. We show that the retrograde p-well effectively addresses the punch-through issue, whilst offering a robust control over the gate threshold voltage. Both the punch-through elimination and gate threshold voltage control are crucial to high-voltage vertical IGBT architectures and are determined by the limits on the doping concentration and depth a conventional p-well implant can have. Without any punch-through, a 10kV SiC IGBT consisting of retrograde p-well yields gate threshold voltages in the range 6-7V with a gate-oxide thickness of 100nm. Gate oxide thickness is typically restricted to 50-60nm in SiC IGBTs if a conventional p-well with $1\times10^{17}cm^{-3}$ is utilized. We further show that the optimized retrograde p-well offers the most optimum switching performance. We propose that such an effective retrograde p-well, which requires low-energy shallow implants and thus key to minimize processing challenges and device development cost, is highly promising for the ultra-high voltage (>10kV) SiC IGBT technology.**

***Index Terms*— SiC IGBTs, Retrograde p-well, Punch-through, Breakdown Voltage, Threshold-voltage control**

I. Introduction

ULTRA-high voltage (>10kV) switching devices, most notably SiC IGBTs, have attracted considerable interest for rapidly emerging sector of applications, such as Smart Grids and HVDC [1-3]. The 10kV class SiC IGBT research has gained significant momentum since the inception of the first 10kV p-IGBT on 4H-SiC in 2005 by Zhang et al, particularly, in the aftermath of realization of high-voltage n-channel devices on free-standing 4H-SiC epilayers in 2010 by Wang et al [4, 5]. Extensive efforts have been put lately on realizing SiC IGBTs in the 10kV-30kV voltage range where they can offer a more favorable trade-off between the conduction and switching losses when compared with unipolar counterparts [6-20].

N-channel IGBTs are generally preferred over P-channel IGBTs and evolved at a rapid pace partially because a positive voltage is required to drive their gate and partially because of exhibiting inherently superior channel mobilities and carrier lifetimes. Although, the processing of n-channel IGBTs is particularly challenging, both the breakdown voltage and specific on-resistance have significantly improved due to important breakthroughs in bulk/epilayer growth and controlled post-process substrate grinding [21]. N-epilayers can be grown as thick as 200µm with a good control on the doping concentration in the range 1×10^{14}-$3\times10^{14}cm^{-3}$ [15-18]. Defect density is acceptable in terms of realizing devices with an active area of 1cm×1cm and the carrier lifetime (τ) is approaching ~12µs [21]. N-channel SiC IGBTs have been successfully demonstrated up to a breakdown voltage of 27kV with continuous improvement in switching characteristics [17-20].

Whilst great emphasis is being placed on the breakdown voltage, a reliable control of the gate threshold voltage (V_{th}) has emerged as a critical issue in the development of ultra-high voltage class (>10kV) of SiC IGBTs [6-20]. A robust control over V_{th} is a prerequisite for a latch-up free and faster IGBT operation.

To have V_{th} in the range 5-7V, a 10kV SiC IGBT requires substantial reduction in the gate oxide thickness (t_{ox}), which in turn leads to long-term reliability issues. Previous studies have shown that the gate oxide thickness is restricted to 50-60nm [4-18]. The doping of conventional p-well can be lowered to further increase the oxide-thickness. However, this makes the IGBT susceptible to issues such as punch-through, latch-up and thus premature electrical breakdown. In the absence of a robust p-well, a high-degree of minority carrier injection, which lowers the junction voltage between the p-well and emitter, can significantly impact the breakdown voltage of IGBTs.

Increasing the depth of p-well is found to be effective for low-voltage devices. However, >10kV devices require the low-doped (~1×10^{17}cm-3) conventional p-well to be >2µm deep. Such an implant depth requires implantation energies in excess of 2.0MeV. High-energy implantations are generally very

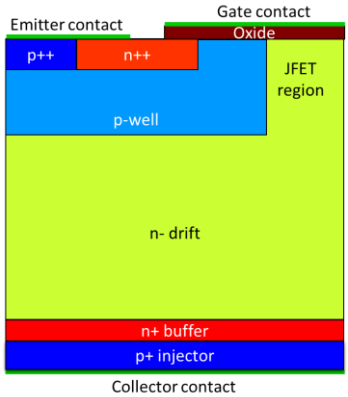

Fig. 1. An n-channel DMOS SiC IGBT

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costly, posing further processing challenges in terms of minimizing the damage to the surface of active area.

Here we present the retrograde approach compatible with ultra-high voltage class of SiC IGBT technology. Retrograde p-well is historically proposed for the high-density Si-based CMOS technology with later studies reporting an improvement in latching performance of scaled devices by the use of specific dopant types, such as Indium, and super-steep doping profile [22-25]. Of late, the retrograde approach is also introduced to SiC devices [3, 5, 8, 26-32]. Most notable efforts include the realization of planar ACCUFET and double-implanted power MOSFETs, being both in 6H-SiC [26, 27].

A few reports are available on the use of retrograde p-well in SiC MOSFETs and IGBTs [3, 5, 8, 28-32]. Nevertheless, little is available in terms of its design requirements and its plausible impact upon the key electrical characteristics of ultra-high voltage SiC IGBTs. The retrograde approach is particularly relevant to >10kV SiC IGBT technology given stringent operational window and considerable processing constraints.

For the first time, retrograde p-well is extensively studied in terms of its impact upon the key electrical characteristics of >10kV class SiC IGBTs. With extensive optimization, we show that it can accommodate blocking voltages as high as 20kV, whilst posing minimal processing challenges. We further show the effectiveness of the optimized retrograde p-well in terms of eliminating punch-through and achieving a robust control on the threshold voltage control by means of depositing thick oxide in ultra-high voltage SiC IGBTs. Thicker gate oxide is crucial to enhance the long-term reliability of power devices, particularly during high-voltage transients or in blocking modes at elevated temperatures. In addition, a thicker gate oxide is also beneficial to reduce the effect of hot carrier degradation and Fowler-Nordheim tunneling, also known as Field Emission. We also show that >10kV SiC IGBT consisting of retrograde p-well offers superior transient performance when compared with counterpart consisting of a conventional p-well.

II. Device Design and Methodology

A two-dimensional DMOS n-IGBT test-cell (Fig. 1), is simulated at room temperature using Technology-Aided Computer Design (TCAD) tools, as embedded in Synopsys-Sentaurus software package. The IGBT test-cell consists of a p^+ anode/injector, n^+ buffer and n^- drift epilayer. The drift epilayer is low-doped and sufficiently thick to support >10kV blocking voltages. The thickness of blocking epilayer for 10kV, 15kV and 20kV designs are 100µm, 150µm and 200µm, respectively. The doping concentration of blocking epilayer for investigated blocking voltages is fixed at $3\times10^{14}cm^{-3}$. The doping concentrations for p^+ anode/injector and buffer epilayer are 1×10^{19} and $1\times10^{18}cm^{-3}$, respectively. Under extensive simulations, the optimized width of JFET region is found to be 5µm and the channel length is fixed at 2µm. The lateral dimensions for regions, such as p^{++} and n^{++} implants underneath the emitter contact, can be chosen as per processing convenience since these do not readily affect the device characteristics investigated here. Material properties of SiO_2 are utilized for the gate oxide.

The lifetimes of carriers are modeled as a product of a doping-dependent, field-dependent and temperature-dependent factors, as embedded in Scharfetter model utilizing Shockley-Read-Hall (SRH) recombination mechanism. Carrier life times of 2.5 µs and 0.5 µs are used of electrons and holes.

Dependency of impact ionization coefficients upon the electric field is calculated using the Okuto-Crowell model. Breakdown characteristics are obtained using a background carrier concentration of 1×10^{9} cm^{-3}.

Caughey-Thomas model is utilized to model doping and temperature dependency of carrier mobility. The dependency of energy bandgap upon both temperature and doping is considered. Incomplete ionization of dopants in 4H-SiC is also considered, being the donor trap of Nitrogen located at 0.0709 eV with respect to the conduction band and the acceptor trap of Aluminum at 0.265 eV with respect to the valance band. Details regarding the simulation models and material parameters are described in our previous work [33-35].

III. Results and Discussion

We begin our investigation by first highlighting the difference between conventional and retrograde p-wells.

A. Retrograde vs. Conventional

The conventional and retrograde p-wells differ mainly in the manner the doping concentration is varied with the depth. Doping profiles for conventional and retrograde p-wells are illustrated in Fig. 2. In a conventional approach, the peak doping concentration of $1\times10^{17}cm^{-3}$ lies mostly at the surface or in the sub-surface region of p-well, which steadily decreases with the depth. In contrast, in the proposed retrograde approach, the doping near the surface or sub-surface region, annotated as region 'a', of the p-well is kept low ($<8\times10^{16}cm^{-3}$), which gradually increases up to 5×10^{17}-$5\times10^{18}cm^{-3}$ in the region

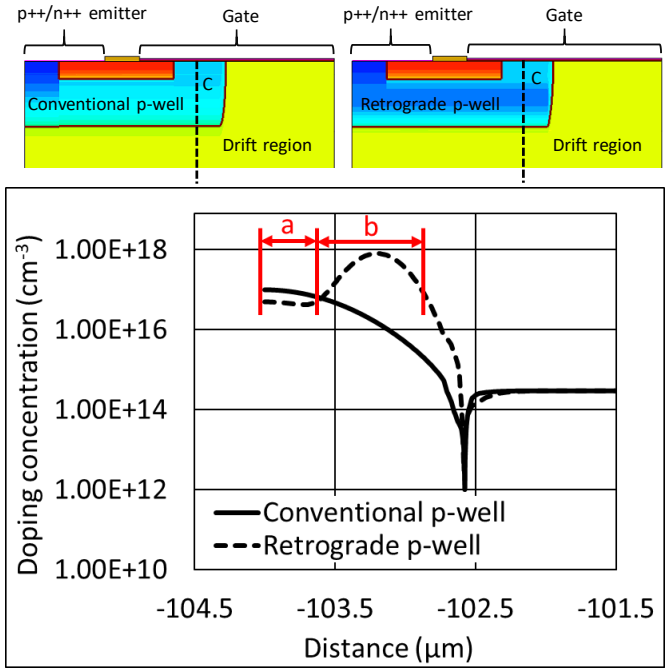

Fig. 2. Illustration of doping profiles along the cut line 'C' for conventional and retrograde p-wells.

annotated as ‘b’ and then begins to decrease with the depth. The low-doping sub-surface region of retrograde p-well is typically 0.2-0.3µm deep, whilst the remaining depth is dedicated to high-doping concentration, typically higher than $5\times10^{17}cm^{-3}$. In this manuscript, the high-doping region (i.e., region ‘b’) is referred as the ‘bottom’ of the retrograde p-well. The retrograde p-well would require two set of implants performed with two separate masks. The region ‘b’ can be realized using the set of high-energy and high-dose implants, whilst region ‘a’ will require the set of low energy-low dose implants.

Next, we examine the performance of an ultra-high voltage (>10kV) SiC IGBT comprising of the retrograde p-well and compare it with that of counterpart comprising of a conventional p-well. We begin with the IGBT blocking characteristics.

B. Blocking characteristics

Simulated breakdown characteristics of a 10kV IGBT cell with conventional and retrograde p-wells are shown in Fig 3. When the conventional design is used, as shown in Fig. 3(a), the collector current rises prematurely at voltages as low as ~400V and at ~6kV for uniform doping of $1\times10^{17}cm^{-3}$ and $3\times10^{17}cm^{-3}$, respectively. Upon increasing the conventional p-well doping from $3\times10^{17}cm^{-3}$ to $5\times10^{17}cm^{-3}$, a desired breakdown occurs, at ~13.5kV, which is very close to the blocking ability of an equivalent 1D open base PNP. It is calculated that same blocking ability can be achieved with doping concentration of $3\times10^{17}cm^{-3}$ but a deeper (~1.5µm) conventional p-well will be required.

In the case of retrograde p-well, the doping concentration at the bottom is intentionally kept at very high level ($>1\times10^{18}cm^{-3}$), which ensures the desired breakdown of ~13.5kV, even if the corresponding highly doped region is relatively thin and shallow. Also, the doping concentration in the sub-surface region, i.e., region ‘a’, of retrograde p-well becomes less important for blocking, which means it can be designed independently. As shown in Fig. 3(b), the sub-surface region doping is allowed to have a wide range of doping concentration, for example, between $5\times10^{16}cm^{-3}$ and $1\times10^{17}cm^{-3}$, with no rapid rise in the current observed. Essentially the retrograde p-well achieves to decouple the blocking ability from the doping of the sub-surface region.

For the case of a conventional p-well, the premature rise in current can be attributed to either punch-through or forward biasing of the p-well/emitter junction during both the on-state and turn-off. The punch-through is caused by the lack of strong depletion barrier at the p-well and drift junction, resulting in a direct current conducting path between the emitter and collector. As elaborated in our previous work [34, 35], the forward biasing of the junction between p-well and emitter can originate from electron-hole pair generation in the high-electric field regions surrounding the p-well. In the case of a high-degree of electron-hole pair generation caused by elevated temperatures, IGBT can also conduct the current in a similar manner.

Under blocking conditions, we have examined profiles of different physical properties, such as, absolute current density, impact ionization, in detail and identified punch-through as the main cause behind premature rapid rise of collector current. Impact ionization is found to be very low, lower than

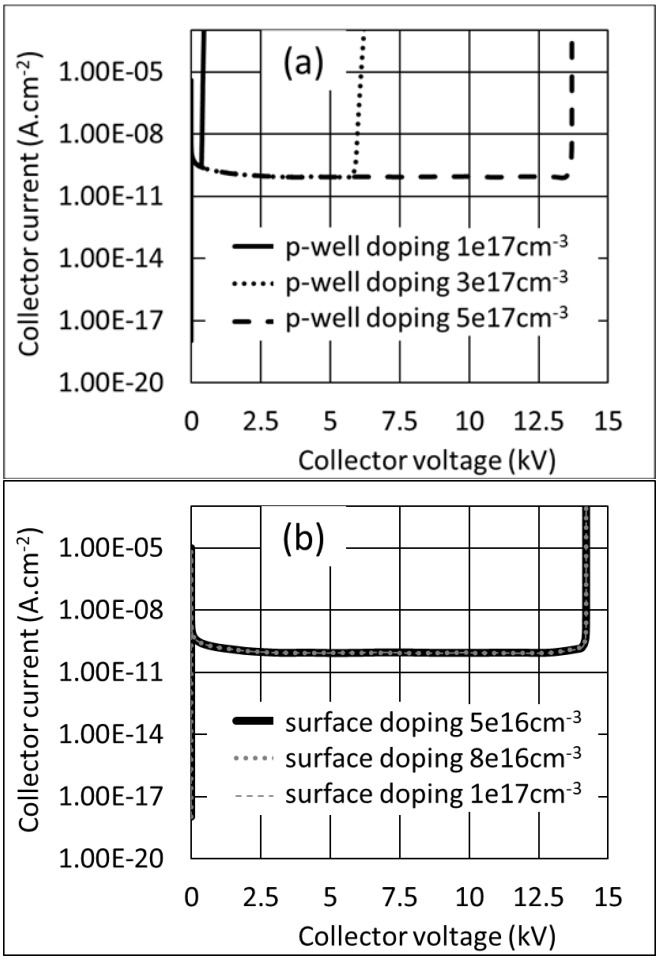

Fig. 3. Blocking characteristics depicting the occurrence of punch-through in a >10kV IGBT cell with (a) a conventional p-well and (b) a retrograde p-well. The value of t_{ox} is 50nm and p-well implants for both conventional and retrograde doping profiles are 0.7-0.8µm deep.

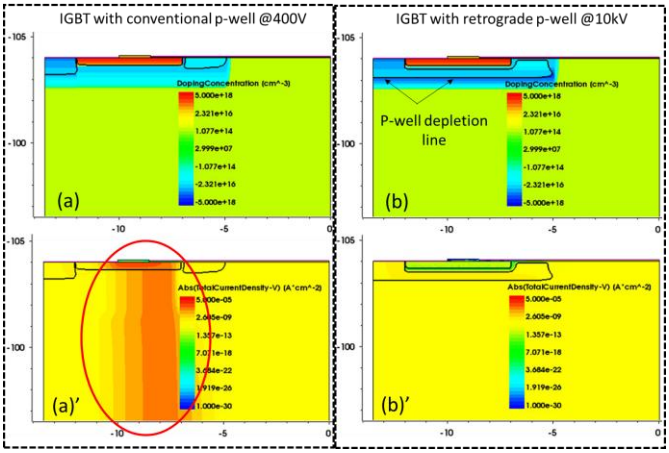

Fig. 4. Depiction of depletion of conventional p-well ((a) and (a’)) and retrograde p-well ((b) and (b’)) just before the rapid rise of collector current. Doping and current profiles for conventional p-well are taken at 400V, while for retrograde p-well these are taken at 10kV. The value of t_{ox} is 50nm and p-well implants are 0.8µm deep. Doping concentrations are $1\times10^{17}cm^{-3}$ for conventional p-well and 5×10^{16} and $3\times10^{18}cm^{-3}$ at the surface and bottom of retrograde p-well, respectively.

$1\times10^{11}cm^{-3}\bullet s^{-1}$ just before the sudden rise of current, i.e., at 400V and 13.5kV for conventional and retrograde p-well IGBT structures.

Absolute current density profiles within IGBTs at different collector voltages are shown in Fig. 4. As shown in Fig. 4 (a), the charge in a 0.8µm deep conventional p-well with doping concentration of $1\times10^{17}cm^{-3}$ is not adequate to hold the depletion from reaching the n^{++} emitter region at 400V. In other words, even at a low-voltage of 400V, the conventional p-well is fully depleted. This is clearly demonstrated in Fig. 4 (a) and (a'): there exists no depletion barrier (solid black line) around the p-well which in turn lets the current to conduct through (red circled region). In contrast, a retrograde p-well with the same depth is only partially depleted at 10kV, consisting of a clear depletion region (depicted by black line) around the retrograde p-well. Indeed, Fig 4 (b) and (b') validate the effectiveness of the retrograde p-well to withstand voltages even higher than 10kV without exhibiting punch-through. This is corroborated by the blocking characteristics of Fig. 3(b), where the SiC IGBT test cell is approaching the maximum theoretical 2D limit of SiC breakdown of ~14kV for drift region thickness of 100µm and doping concentration of $3\times10^{14}cm^{-3}$.

C. Further design considerations for 10-20kV range

To achieve blocking ability higher than 10kV, as high as 20kV, the total charge in the p-well needs to be increased. As depicted in Fig. 5, to achieve 10kV using a conventionally designed p-well, the doping needs to be higher than $3\times10^{17}cm^{-3}$ and p-well depth of ~1.5µm. Alternatively, one can reduce the p-well depth to 0.6-0.8 µm but this would require a doping concentration higher than $8\times10^{17}cm^{-3}$. For 20kV blocking ability, even deeper p-wells are needed. In contrast, the retrograde profile can be optimized to block voltages higher than 10kV with a total depth of as thin as 0.6-0.7µm and bottom doping density of $>1\times10^{18}cm^{-3}$. The same depth is found to be adequate to block 20kV but with slightly higher doping density requirement of $>3\times10^{18}cm^{-3}$. These results are shown in Fig. 6 (a) and (b). The results for the retrograde case indeed demonstrate a remarkable improvement over the equivalent conventional p-well, which needs to be deeper than 1.5µm for ultra-high voltage IGBTs.

To mitigate from the adverse effect of electric field crowding

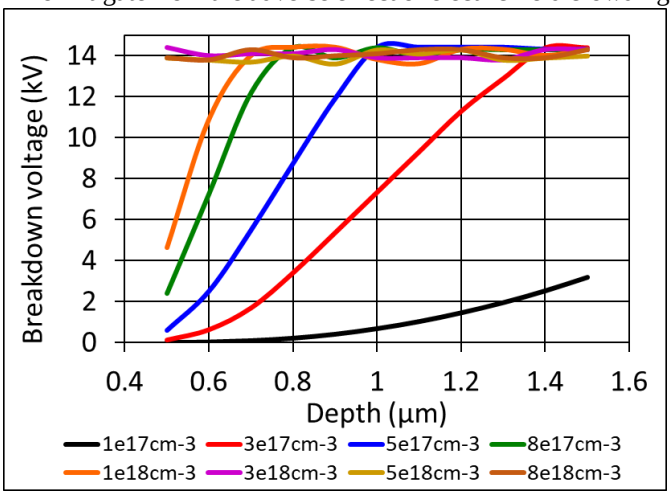

Fig. 5. Optimization of the doping concentration and depth of a conventional p-well for 10kV SiC IGBT.

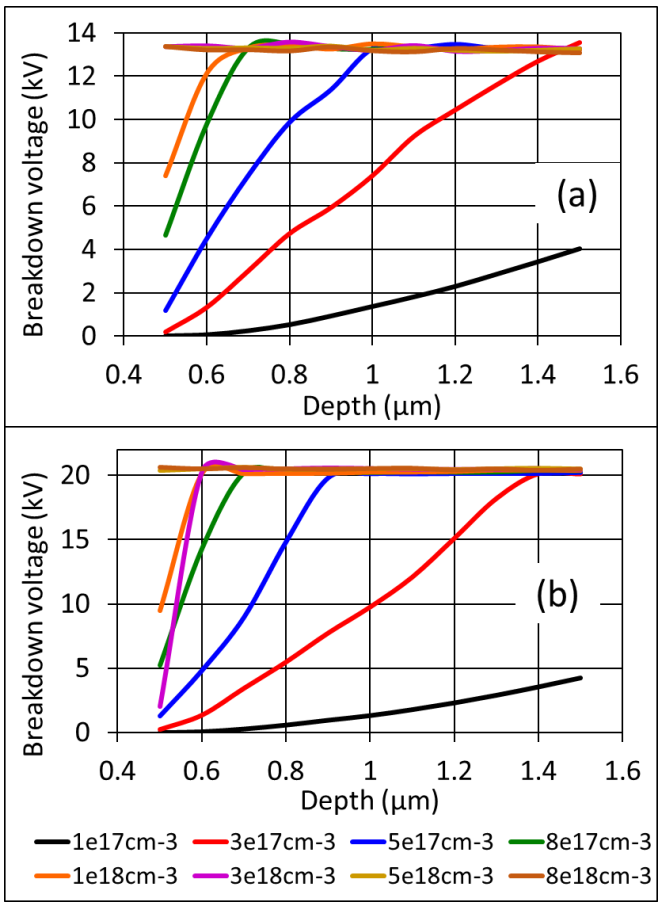

Fig. 6. Optimization of the doping concentration and depth of the retrograde p-well for (a) 10kV and (b) 20kV SiC IGBTs.

at the curvature and the equivalent enhanced impact ionization, the exact profile of the region has been optimised accordingly. This is particulalry important for voltages higher than 10kV. Towards this direction the bottom ~0.2µm of the total retrograde p-well depth is designed to be lowly doped. Also, the high-doping region within the p-well is kept away from the corner. The optimized design essentially achieves a softer junction at the bottom and the corner of the p-well and therefore reduces effectively the curvature of the electrostatic distribution and the electric field crowding observed during blocking. It has also been achieved to avoid degradation of the IGBT blocking voltage when the peak doping concentration of the retrograde p-well increases. The latter is key requirement for achieving blocking voltages 10-20kV. For example, as shown in Fig. 6 (a), the blocking voltage remains constant at 13.5kV, even when the doping concentration at the bottom of the p-well is increased to $8\times10^{18}cm^{-3}$. For ultra-high voltage IGBTs these design considerations become necessary when aiming to achieve the maximum possible breakdown voltage without the use of costly deep implantations.

D. Threshold voltage control

The gate-oxide thickness is an important design parameter which strongly affects V_{th}. Fig. 7 shows the calculated V_{th} as a function of t_{ox} for different values of doping concentrations used in conventional and retrograde p-wells. As can be seen in Fig. 7(a), for a conventional p-well of doping concentration $1\times10^{17}cm^{-3}$, 60nm is the maximum allowable t_{ox} to ensure V_{th}

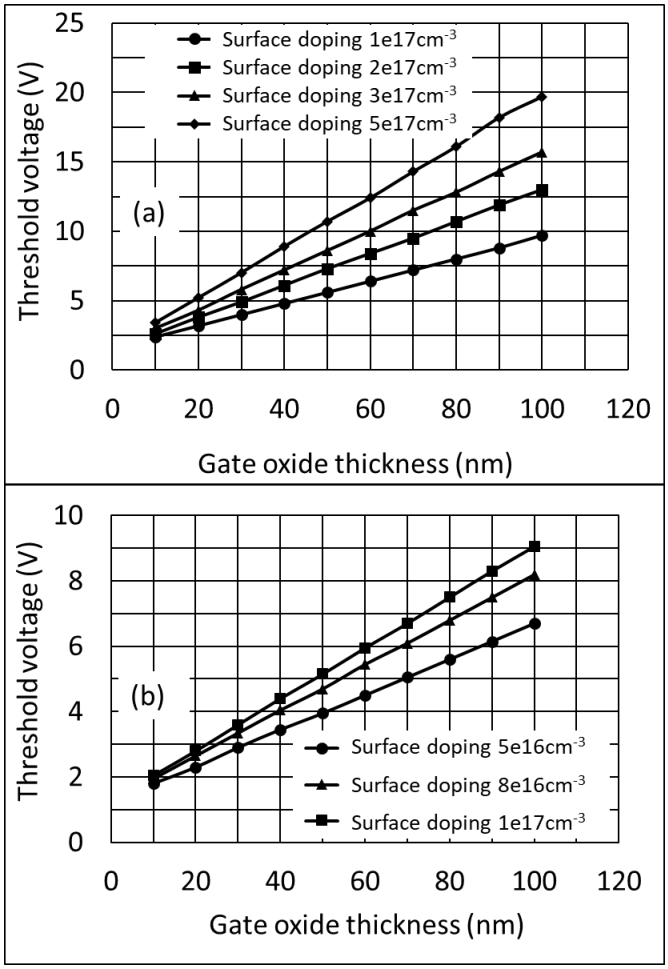

Fig. 7. Calculated V_{th} for a >10kV SiC IGBT as a function of t_{ox} for different values of doping (a) in a conventional p-well and (b) at the surface of a retrograde p-well. The bottom of retrograde p-well is fixed at ~1×10^{18}cm^{-3}. The region of interest for V_{th} of a SiC IGBT lies between 5V and 7V.

below 7V. If higher doping concentrations are used, e.g. to enable blocking ability of 10kV, the value of the maximum allowable t_{ox} is even smaller than 50nm. With the introduction of the retrograde p-well, the allowable gate oxide thickness increases dramatically. A gate threshold voltage of less than 7V can be achieved with oxide layers being as thick as 100nm. Since the sub-surface doping concentration in a retrograde p-well does not affect the blocking ability, there is an extra degree of freedom. As shown in the previous subsection, if required, the doping of the p-well region closer to the surface can be lower than 5×10^{16}cm^{-3} in order to allow for a gate oxide thicker than 100nm. For a doping concentration of 1×10^{16}cm^{-3}, one can utilize 150nm gate oxide without surpassing V_{th} of 7V.

E. Switching characteristics

Whilst the advantage of having a retrograde p-well in ultra-high voltage SiC IGBTs is evident in the static performance, it is instructive to access its impact upon the switching performance and to compare it with that of a conventionally doped. The turn-off waveforms of 10kV rated SiC IGBTs consisting of retrograde and conventional p-well are assessed for their switching performance under inductive load conditions, as illustrated in Fig. 8. The DC link voltage is set to 6kV and load resistance set at 120Ω, yielding the current

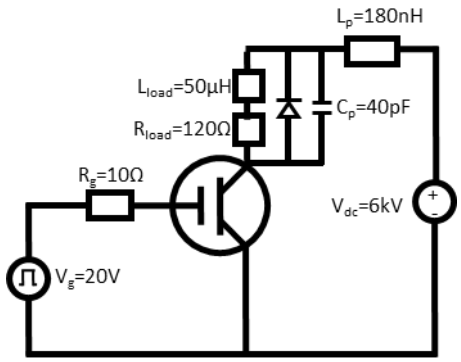

Fig. 8. Circuit schematic used in mixed-mode simulations of inductive load turn-off of 10kV SiC IGBTs.

density of 50A•cm^{-2}. The gate voltage applied is set to 20V, which is well above the threshold voltage of all design variations assessed.

As shown in Fig. 9 (grey lines), an IGBT with conventional p-well doped 1×10^{17}cm^{-3} and with depth of 1.3-1.5μm is grossly inadequate to achieve good turn-off characteristics. Turn-off behavior is improved with increased in doping concentration of conventional p-well, however, this is coming at the cost of significant increase in the gate threshold voltage.

To assess the effect of the retrograde p-well IGBT and to optimize its profile for the most optimum IGBT switching behavior, a large number of design variants are investigated. Even for the retrograde p-well, a higher doping concentration and greater depth is desirable in terms of efficient extraction of holes through the p-well. However, there is limit to what can realized in practice. We have further examined the impact of both the depth and bottom doping of retrograde p-well. As shown in Fig. 10 (a), the turn-off behavior of 10kV SiC IGBT improves with an increasing depth of the retrograde p-well. However, even a shallow retrograde p-well with depth of 0.8μm and bottom with doping of 1×10^{18}cm^{-3}, yields excellent turn-off behavior. The turn-off time is low, lying in the range 550-600ns.

As shown in Fig. 6(a), a doping concentration of 5×10^{17}cm^{-3} at the bottom of the retrograde p-well is adequate to reach 10kV blocking capability. However, in transient simulations at 6kV (Fig. 9b), 5×10^{17}cm^{-3} exhibits a very large turn-off time of

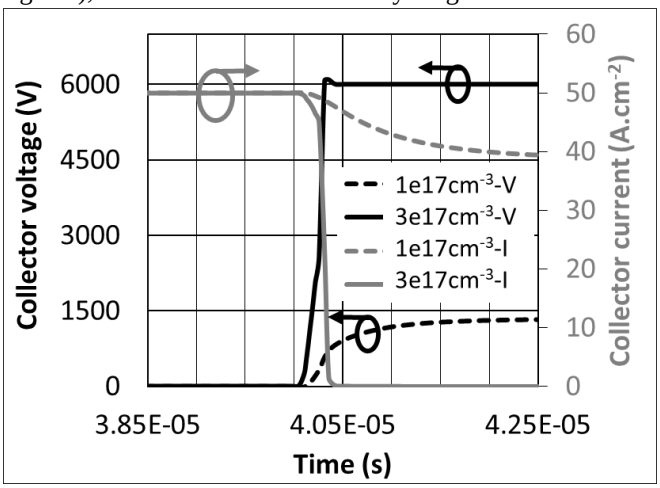

Fig. 9. Inductive load turn-off in a >10kV SiC IGBT with conventional p-well. The p-well depth is fixed at 1.3-1.5μm. The gate-oxide thickness is 50nm.

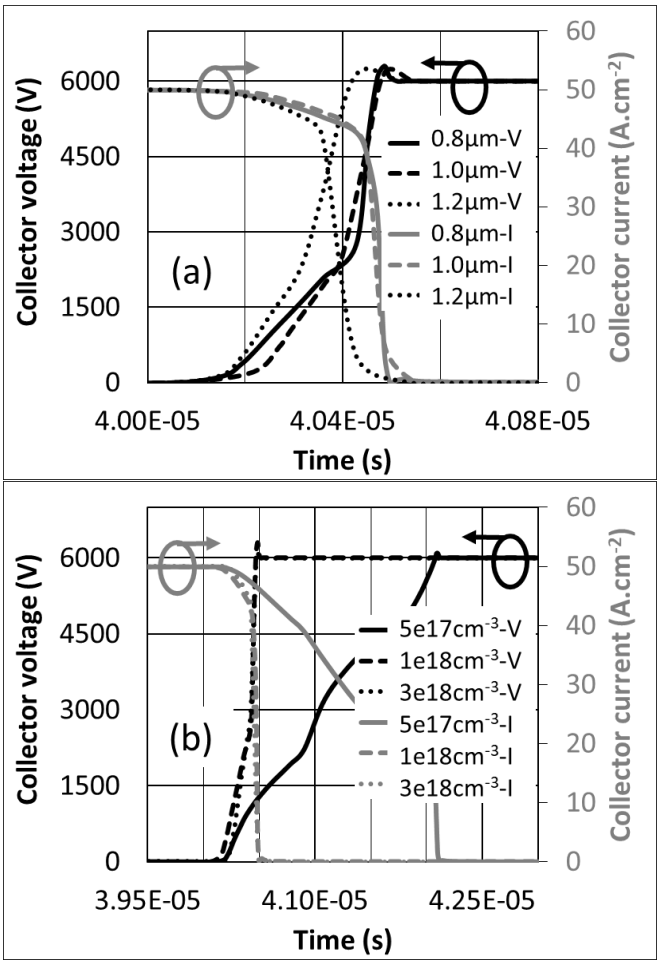

Fig. 10. Inductive load turn-off in a >10kV SiC IGBT with retrograde p-well. (a) Effect of p-well depth and (b) effect of p-well doping. The p-well bottom-doping in (a) is fixed at 1×10^{18}cm^{-3} and in (b) depth is fixed at 0.8 µm. The doping concentration at the surface of retrograde p-well is fixed at 5×10^{16}cm^{-3} with 50nm gate-oxide lying on top it.

1.5µs. Such a large turn-off time is likely to amount to considerable losses and possibly leading to an IGBT failure. This is an important design consideration, while utilizing retrograde p-wells in ultra-high voltage SiC IGBTs. The turn-off time has been considerably reduced with increased doping at the bottom of retrograde p-well. However, for doping concentrations higher than 1×10^{18}cm^{-3}, there is not much improvement in switching characteristics.

We have further accessed turn-off losses. We find that >10kV SiC IGBT consisting of the optimized retrograde p-well, i.e., sub-surface doping 5×10^{16}cm^{-3}, bottom doping 1×10^{18}cm^{-3} and depth 0.8 µm, exhibits nearly three order of magnitude lower losses of 4.83×10^{-5} J•cm^{-2} in comparison to 2.15×10^{-2} J•cm^{-2} of the counterpart consisting of a conventional p-well with uniform doping of 3×10^{17}cm^{-3} and depth 1.5 µm.

IV. Conclusion

In conclusion, we have investigated the effect of retrograde p-well doping profile upon the key characteristics of 10kV-class SiC n-IGBTs. Under extensive simulations, we showed that the retrograde p-well eliminates the possibility of a premature breakdown due to punch-through even when a shallow implantation depth of <1µm is adopted. Reduction in implantation energies is crucial to cut the fabrication cost.

We have further showed that the doping concentration of the sub-surface region of the retrograde p-well does not affect the blocking ability, and hence it can be varied over a very large range to achieve a desirable control over V_{th} by means of oxide deposition. An appropriately doped sub-surface region of the retrograde p-well, for example, $<1\times10^{16}$cm^{-3}, is allowing the use of gate oxides thicker than 100nm, whilst yielding V_{th} in the range of 5-7V. An extended control on V_{th} with thicker oxide offers processing convenience and is particularly beneficial to address issues arising 'oxide-reliability' and phenomena such as Fowler-Nordheim tunneling and hot carrier injection.

It is worth mentioning here that a substantial reduction in the sub-surface doping, which has been possible only because of the retrograde approach, can further help with improving the channel mobility of SiC MOS devices. Kimoto *et al.* have previously reported on increase in the channel mobility with decreasing p-body doping concentration for different crystal faces. Channel mobilities increased from 12 to 26cm^2•V^{-1}•s^{-1}, and 61 to 78cm^2•V^{-1}•s^{-1} on the Si 0001 and 1$\bar{1}$21 faces, respectively, when the acceptor doping concentration of p-body decreased from 2×10^{17} to 1×10^{16}cm^{-3} [36]. Of particular interest is the channel mobility of 145cm^2•V^{-1}•s^{-1} obtained by Ortiz *et al.* using a very low acceptor concentration of 1×10^{15}cm^{-3} on the 0001 Si-face [37]. Previously, Katakami et al. showed an improvement in the channel mobility of p-channel SiC IGBT using the combination of adopting an n-type base layer with a retrograde doping profile and additional wet re-oxidation annealing (wet-ROA) at 1100°C in the gate oxidation process. Considering such a large degree of freedom a designer can have over the selection of doping near the channel region, the retrograde p-well possesses significant importance to the SiC-based MOS technology.

In terms of transient performance, we find that the exact doping profile of retrograde p-well can affect the turn-off speed and losses. We note that the retrograde p-well with depth of 0.8µm and a peak concentration of 1×10^{18}cm^{-3} at its bottom gives the most optimum switching performance.

We therefore propose that the retrograde p-well is a highly promising approach for ultra-high voltage (>10 kV) SiC IGBTs. The retrograde p-well concept possesses scope beyond SiC IGBTs, covering a diverse range of MOS-based power devices, such as, MOSFETs and IGCTs on advanced materials, such as, diamond and Ga_2O_3, where the implantation process is particularly challenging.

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