TCAD modelling of current dispersion in a 0.25 µm gate length GaN HEMT

Faramehr, S., Igic, P. & Kalna, K.

Original citation & hyperlink:
Faramehr, S, Igic, P & Kalna, K 2013, TCAD modelling of current dispersion in a 0.25 µm gate length GaN HEMT. in The Ninth International Conference on Advanced Semiconductor Devices and Mircosystems . IEEE, pp. 11-14, The Ninth International Conference on Advanced Semiconductor Devices and Mircosystems, Smolenice, Slovakia, 11/11/12.
https://dx.doi.org/10.1109/ASDAM.2012.6418566

DOI 10.1109/ASDAM.2012.6418566
ISBN 978-1-4673-1198-4

Publisher: IEEE

TCAD Modelling of Current Dispersion in a 0.25 µm Gate Length GaN HEMT

S. Faramehr, P. Igić and K. Kalna

Electronic Systems Design Centre, College of Engineering,
Swansea University, Singleton Park, Swansea, SA2 8PP, Wales, United Kingdom
E-mail: 476599@swansea.ac.uk

Current dispersion due to acceptor-type defects acting as electron traps are studied using 2D TCAD transient simulations. High and low drain pulse voltages are applied to study a dynamic picture of trapping and de-trapping of electrons using Drift Diffusion and Hydrodynamic transport models. In addition, Schottky electron tunnelling is employed to transient simulations in the presence of different densities of traps in the barrier to investigate how tunnelling affects the drain current at off-state.

1. Introduction

Gallium nitride high electron mobility transistors (GaN HEMTs) are ideal candidates for power electronic applications from power conditioning to microwave amplifiers and transmitters thanks to unique properties of III-N materials such as wide bandgap, high breakdown voltage, and good thermal dissipation [1-14]. The spontaneous and piezoelectric polarizations present in III-N materials can result in a 2D electron gas (2DEG) density in the channel above 10^{13} cm^{-2} [3, 5, 7, 10]. While GaN HEMTs have demonstrated an excellent performance, the greatest challenge remains to achieve a high level of reliability and stability concurrently with the device performance [3]. Improvement in reliability needs understanding of the failure mechanisms. Among the limiting factors affecting reliability of GaN HEMTs, the current collapse is the most critical issue.

The current collapse is a temporary reduction of drain current after the application of high voltage [2, 4, 6, 8]. In DC measurements, this phenomenon manifests itself as a reduction in the drain current [5]. In RF applications, the current collapse limits RF performance compared to what is expected from the DC characterization [2, 4]. This phenomenon also limits the output power densities in GaN HEMTs. Several reports suggest that the surface trapping and the bulk trapping play important roles as the parasitic charge trapped on the surface or in the device body modifies the density of 2DEG in the channel and limits switching characteristics of the device [2, 6, 7]. Dispersion effects caused by the surface traps can be minimized by surface passivation [8], while minimizing or eliminating dispersion effects caused by the bulk traps is still in question as there is not widely accepted explanation for the nature and location of the traps generated in GaN HEMTs [9].

In previous works, effects of donor-type surface traps and acceptor-type bulk traps using pulsed techniques were studied in GaN HEMTs [10, 11, 12]. However, the gate tunnelling has not been included and its effect on the leakage current has been ignored. In this paper, the buffer trapping and de-trapping of hot electrons are modelled using Atlas simulation toolbox by Silvaco. Direct electron tunnelling through the Schottky barrier is taken into account using Tsu-Esaki model [13]. The current collapse phenomenon and the effect of electron tunnelling on the leakage current is modelled and discussed. Traditionally, the current collapse is measured with pulsed techniques in sub-microsecond range [4]. The same range is therefore employed in this work.

2. Physical and Simulation Models

Figure 1 represents a schematic of the modelled GaN HEMT. The top $Al_{0.28}Ga_{0.72}N$ layer and GaN buffer thicknesses of the device are 21 nm and 1.9 µm, respectively. The source, gate and drain contact lengths are assumed to be 0.25 µm. The spacing between the source to the gate and the gate to the drain are 1.25 µm and 2.50 µm respectively.

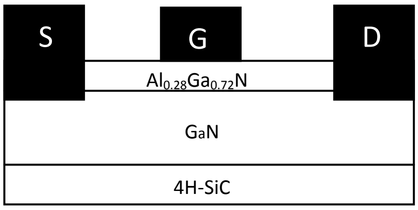

Fig. 1. Cross section of the simulated 0.25 µm gate length GaN HEMT.

Figure 2 illustrates the net polarization charge in a GaN HEMT. The spontaneous and piezoelectric polarization charge components in the AlGaN/GaN HEMTs are calculated using following relations [14]:

$$P_{SP}(x)=(-0.052\cdot x-0.029)\ [C\ m^{-2}] \quad (1)$$

$$P_{PZ}=2\,\frac{a-a_0}{a_0}\left(e_{31}-e_{33}\frac{C_{13}}{C_{33}}\right)\ [C\ m^{-2}] \quad (2)$$

In Eq. (2), C_{13} and C_{33} denote the elastic constants, and a and a_0 are the lengths along the hexagonal crystallographic edge. For the lattice, elastic, and piezoelectric constants, the following relations are used [14]:

$$a_0(x)=(-0.077\cdot x+3.189).10^{-10}\ [m] \quad (3)$$

$$C_{13}=(5\cdot x+103)\ [GPa] \quad (4)$$

$$C_{33}=(-32\cdot x+405)\ [GPa] \quad (5)$$

$$e_{33}(x)=(0.73\cdot x+0.73)\ [C\ m^{-2}] \quad (6)$$

$$e_{31}(x)=(-0.11\cdot x-0.49)\ [C\ m^{-2}] \quad (7)$$

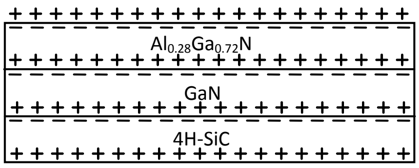

Fig. 2. Scheme of charge components in a GaN HEMT.

Note that the both spontaneous and piezoelectric polarizations are included in the simulation model. Material parameters used in simulations are summarised in Table I. The sheet charge density of $\sigma_{pol}=1.15\times10^{13}$ cm^{-2} that is obtained at the interface of AlGaN/GaN is in agreement with the experiments.

Table I. Room-temperature values for III-Vs material adopted in the simulations [14].

Material Properties	GaN	AlN
Bandgap [eV]	3.47	6.2
SRH Life Time [ns]	1	1
Electron Relaxation Time [ps]	0.1	0.1
Low-Field Electron Mobility [Cm^2/Vs]	990	135
Electron Saturation Velocity [Cm/s]	1.8×10^7	2.16×10^7

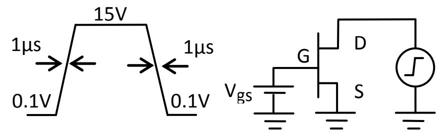

Fig. 3. Drain turn-on and turn-off pulsing modes.

The current collapse has been widely attributed to the trapping phenomena [1-12]. The trapping centres can reside in AlGaN barrier layer, at the 2DEG interface, or in the GaN buffer layer [6, 14]. To investigate trapping behaviour in the simulated device, two acceptor-type traps are uniformly distributed in the AlGaN and GaN layers with a density of $N_T^{AlGaN}=5\times10^{16}$ cm^{-3} and $N_T^{GaN}=2.5\times10^{16}$ cm^{-3}, respectively. The position of the traps in AlGaN and GaN layers are assumed to be E_C-E_T = 2.5 eV and E_C-E_T = 1.25 eV, respectively. The capture cross section of electrons in AlGaN and GaN layers is assumed to be σ_n= 5×10^{-15} cm^{-2}. Poisson equation, a continuity equation, Shockley-Read-Hall recombination model, and the tunnelling model are all included in the simulations. The simulations are carried out using two transport models: Drift-Diffusion (DD) and Hydro-Dynamic (HD) which were meticulously calibrated against experimental I-V characteristics (I_{ds}-V_{ds} at V_{gs}=-2V, -1V, 0V) of the 0.25 µm gate length GAN HEMT [5]. The lattice temperature is fixed in all simulations to 300 K°.

3. Transient Simulations

Figure 4 represents the simulated transient response to V_{ds} turn-on pulse at V_{gs}=0V using the HD transport model. The current decline can be split into two regimes. In the first regime, the decline is caused by two effects: 1) negative differential mobility which is a dominant effect and 2) electron trapping into the acceptor traps. The negative differential mobility is not observed in the DD model. The recovery time of negative differential mobility is short in comparison to the recovery time required by the traps (see Fig. 4). In the second regime, the decline is caused by the capture of hot electrons into traps. Some of the empty acceptor traps, which are neutral, capture electrons and become negatively charged. This process is called trapping. On the other hand, some of the filled acceptor traps, which are negatively charged, emit electrons and become neutral. This process is called de-trapping [15]. Trapping and de-trapping processes are dynamic but one could be dominant until the system reaches equilibrium conditions. When V_{ds} is ramped up from 0.1V to 15V, electrons are significantly heated in 10^{-6} s, and system finds itself far from equilibrium conditions. As a result, hot electrons exit the channel and spread toward AlGaN and GaN layers and get captured by the traps in the device. Captured electrons modify the charge distributions in the device, thereby limiting the output power. Meanwhile, small numbers of the trapped electrons can lose energy and return to the channel. When the drain voltage is ramped up, the trapping behaviour is the dominant process [see Fig. 6(a)].

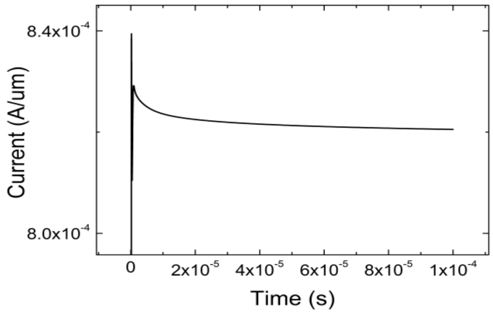

Fig. 4. Simulated transient response to V_{ds} ramp-up pulse at V_{gs}=0V and V_{ds}=0.1V using the HD transport model.

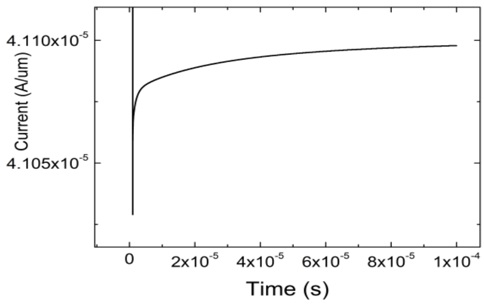

Fig. 5. Simulated transient response to V_{ds} ramp-down at V_{gs}=0V and V_{ds}=15V using the HD transport model.

(a)
(b)

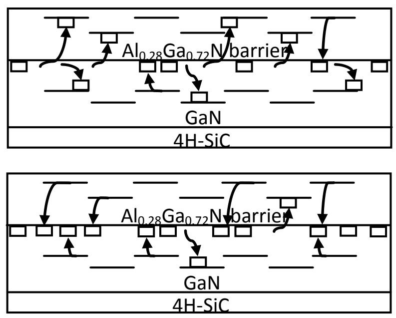

Fig. 6. Schematic illustration of electron capture/emission process for (a) turn-on pulse at V_{gs}=0V and V_{dd}=15V and (b) turn-off pulse at V_{gs}=0V and V_{dd}=0.1V.

Figure 5 shows the simulated transient response to V_{ds} turn-off pulse at V_{gs}=0V using the HD transport model. When V_{ds} is ramped down from 15V to 0.1V in 10^{-6} s, once again system finds itself far from equilibrium conditions. Consequently, the occupied traps start to release the electrons. This behaviour determines the de-trapping process. Meanwhile, a very small number of electrons could be heated and get trapped. When the drain voltage is pulsed down, the de-trapping behaviour is the dominant process [see Fig. 6(b)].

Figure 7 illustrates the simulated transient response to V_{ds} turn-on pulse at V_{gs}=-5V (off state) using the DD model with tunnelling included/excluded. When V_{ds} is ramped up from

0.1V to 20V in 10^{-6} s, the current shortly increased by about two orders of magnitude. During the transient evolution, a noticeable decline is observed as the system finds itself in non-equilibrium conditions. As it is shown in Fig 7, the leakage current is increased when tunnelling model is included. This corresponds to increase in number of electrons under the gate. Fig. 8 shows the leakage current plotted for different values of acceptor trap densities in the AlGaN layer and compared to the case with no tunnelling. The current decreases with increasing trap density due to increase in the electron trapping as expected.

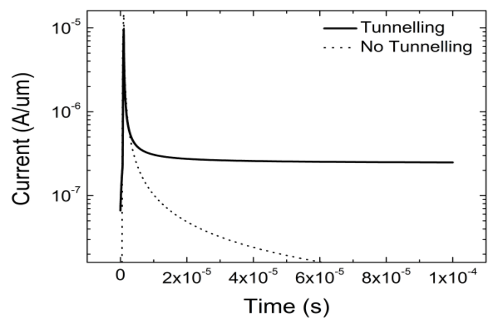

Fig. 7. Simulated transient response of the drain current at V_{ds}=20V and V_{gs}=-5V with and without a tunneling using the DD transport model. The trap density is $5\times10^{16}cm^{-3}$.

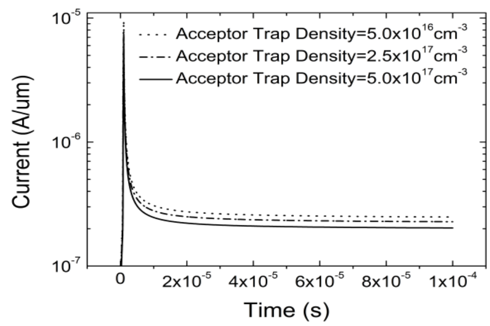

Fig. 8. Simulated transient response of the drain current at V_{ds}=20V and V_{gs}=-5V for different acceptor trap densities in the barrier layer with a tunneling using the DD transport model.

4. Conclusion

Despite of promising performance of GaN HEMTs for power applications, further investigation and development of this technology regarding optimisation of material quality and process technology to eliminate or, at least, minimize the prominent issue of the traps is required. This work presented an insight into the bulk trapping process in the 0.25 μm GaN HEMT through the physical device modelling of the acceptor traps in on-state and off-state device regimes. We have observed that the electron tunnelling will increase the trapping process by order of magnitude in the current characteristics when the device operates in the off-state. However, in the on-state, the tunnelling has negligible impact on the trapping process.

References

[1] S. DasGupa, et al., *IEEE Trans. Electron Devices*, **59**, 2115-2122 (2012).
[2] J. Joh, et al., *IEEE Trans. Electron Devices*, **58**, 132-140 (2011).
[3] G. Meneghesso, et al., *IEEE Trans. Device Mater. Rel.*, **8**, 332-343 (2008).
[4] J. Joh, et al., *IEEE Electron Device Lett.* **29**, 665-667 (2008).
[5] S. Faramehr, et al., *Proc. Microelectronics (Miel)*, 233-236 (2012).
[6] S. C. Binari, et al., *Proc. IEEE*, **90**, 1048-1058 (2002).
[7] O. Mitrofanov, et al., *Appl. Phys. Lett.* **84**, 422-424 (2004).
[8] R. Ventury, et al., *IEEE Trans. Electron Devices*,**48**, 560-566 (2001).
[9] M. Ťapajna, et al., *IEEE Electron Device Lett.* **31**, 662-664 (2010).
[10] J. M. Tirado, et al., *Semicond. Sci. Technol*, **21**, 1150-1159 (2006).
[11] W. D. Hu, et al., *J. Appl. Phys*, **105**, 084502-084502-7 (2009).
[12] A. Chini, et al., *IEEE Electron Device Lett*, **30**, 1021-1023 (2009).
[13] R. Tsu and L. Esaki, *J. Appl. Phys.* **22**, 562-564 (1973).
[14] R. Quay, *Gallium Nitride Electronics*, Springer, Germany, 2008.
[15] P. Ransom, et al., *Proc. Phys. Soc.*, **67**, 646-650 (1954).