Viable 3C-SiC-on-Si MOSFET design disrupting current Material Technology Limitations

Arvanitopoulos, A., Antoniou, M., Li, F., Jennings, M. R., Perkins, S., Gyftakis, K. N. & Lophitis, N.

Original citation & hyperlink:
Arvanitopoulos, A, Antoniou, M, Li, F, Jennings, MR, Perkins, S, Gyftakis, KN & Lophitis, N 2019, Viable 3C-SiC-on-Si MOSFET design disrupting current Material Technology Limitations. in 2019 IEEE 12th International Symposium on Diagnostics for Electrical Machines, Power Electronics and Drives (SDEMPED). IEEE, pp. 364 - 370, IEEE 12th International Symposium on Diagnostics for Electrical Machines, Power Electronics and Drives, Toulouse, France, 27/08/19.
https://dx.doi.org/10.1109/DEMPED.2019.8864910

DOI 10.1109/DEMPED.2019.8864910
ISBN 978-1-7281-1832-1

Publisher: IEEE

Viable 3C-SiC-on-Si MOSFET design disrupting current Material Technology Limitations

A. Arvanitopoulos, M. Antoniou, F. Li, M. R. Jennings, S. Perkins, K. N. Gyftakis and N. Lophitis

***Abstract* — The cubic polytype (3C-) of Silicon Carbide (SiC) is an emerging semiconductor technology for power devices. The featured isotropic material properties along with the Wide Band Gap (WBG) characteristics make it an excellent choice for power Metal Oxide Semiconductor Field Effect Transistors (MOSFETs). Nonetheless, material related limitations originate from the advantageous fact that 3C-SiC can be grown on Silicon (Si) wafers. One of these major limitations is an almost negligible activation of the p-type dopants after ion implantation because the annealing has to take place at relatively low temperatures. In this paper, a novel process flow for a vertical 3C-SiC-on-Si MOSFET is presented to overcome the difficulties that currently exist in obtaining a p-body region through implantation. The proposed design has been accurately simulated with Technology Computer Aided Design (TCAD) process and device software and a comparison is performed with the conventional SiC MOSFET design. The simulated output characteristics demonstrated a reduced on-resistance and at the same time it is shown that the blocking capability can be maintained to the same level. The promising performance of the novel design discussed in this paper is potentially the solution needed and a huge step towards the realisation of 3C-SiC-on-Si MOSFETs with commercially grated characteristics.**

***Index Terms* — MOSFETs, 3C-SiC-on-Si, TCAD, SRIM, Silicon Carbide, Wide Band Gap**

I. Introduction

Silicon Carbide (SiC) is a wide band gap (WBG) semiconductor material with superior material characteristics compared to silicon (Si). Due to that, devices based on this material are expected to replace their Si counterparts in power electronic applications. These WBG properties include at least two times wider energy bandgap, an order of magnitude higher critical electric field (E_{cr}) and largely improved thermal conductivity.

A. Arvanitopoulos, Faculty of EEC at Coventry University, Coventry, UK (e-mail: arvanita@uni.coventry.ac.uk).

M. Antoniou, School of Engineering, University of Warwick, Coventry, UK (e-mail: ma308@cam.ac.uk).

F. Li, School of Engineering, University of Warwick, Coventry, UK (e-mail: f.li.3@warwick.ac.uk).

M. R. Jennings, College of Engineering, Swansea University, Swansea, UK (e-mail: m.r.jennings@swansea.ac.uk).

S. Perkins, Faculty of EEC at Coventry University, Coventry, UK (e-mail: perkin19@uni.coventry.ac.uk).

K. N. Gyftakis, School of Engineering, University of Edinburgh, UK, (e-mail: k.n.gyftakis@ieee.org).

N. Lophitis, Faculty of EEC at Coventry University, Coventry, UK (e-mail: n.lophitis@coventry.ac.uk).

The SiC can be polymerized in numerous polytypes, nonetheless only one cubic (3C-) phase of SiC exists. The isotropic characteristics of 3C-SiC [1][2] in conjunction to its remarkable thermal conductivity makes it a prime option for WBG power devices. The cubic SiC can be hetero-epitaxially grown on Si substrates using CVD [3]. This enables for large 3C-SiC-on-Si crystals, that match the diameters of commercially available Si wafers [4]. In consequence, discrete power devices of reduced cost can be obtained. Furthermore, the interest in the monolithic integration of SiC devices with Si technology makes the 3C-SiC an excellent WBG semiconductor for power devices.

The 3C-SiC is particularly promising for MOSFETs, although it features a smaller bandgap value compared to the two other major hexagonal SiC polytypes (4H-, 6H-) [5]. It has been shown that a 3C-SiC MOS-based switch demonstrates less switching losses compared to a 4H-SiC MOS-based switch with the same blocking capabilities [6]. Further, its smaller critical electric field value has been proven beneficial for high frequency MOSFETs [7]. Notably, due to the narrower bandgap energy window of 3C-SiC, the majority of the observed SiO_2/SiC interface trap are energetically located in the conduction band (E_C), essentially improving the effective channel mobility [8]–[11].

Both vertical and lateral 3C-SiC-on-Si power MOSFETs have been developed and characterized in the literature [12]–[17]. However, they are not commercialized yet because of the high planar defects density in the 3C-SiC grown layers originating from the hetero-interface to Si during growth [18]. Currently, this is the main bottleneck for the 3C-SiC-on-Si material technology that hinder its anticipated device performance potential.

It has been demonstrated that the density of the SiO_2/3C-SiC-on-Si interface states (D_{it}) heavily depends on the quality of the initial epilayer [19]. The volume of the formed planar defects can be reduced when 3C-SiC is grown on undulant-Si substrates [4]. In [5], MOS capacitors fabricated on a 3C-SiC-on-Si surface after ultra-violet (UV) irradiation/ozone cleaning, had their SiO_2/SiC interface properties greatly improved. It is also reported that a shallow Nitrogen (N) implantation at the gate oxide region prior to the thermal oxidation reduces the D_{it} [20]. Therefore, improvements of the 3C-SiC heteroepitaxy set

the premises on delivering significantly more reliable MOS structures.

Interestingly, one of the 3C-SiC beneficial properties, the ability to grow on cheap and large diameter Si substrates also raises another challenge for this technology in terms of p-type doping. Boron (B) and Aluminium (Al) are two of the most preferable p-type dopants for 3C-SiC. However, the B is linked with the formation of deep energy levels in the SiC [21]. At the same time, the physical similarities of Al and Si in terms of atomic size and masses prevents lattice distortions that can act as scattering centres. Thus, Al is the main option for planar selective area doping for the formation of p-type region in the 3C-SiC material.

The Si substrate limits the activation temperature of the acceptor type implanted dopants in 3C-SiC below its melting point. This value of approximately 1350°C is further down compared to the required annealing temperatures of Al, which can be as high as 1700°C for a nearly perfect activation (>95%) [22]. In consequence, p-type regions by ion implantation is difficult to achieve.

The challenging nature of acceptor activation is also highlighted in [23], where 3C-SiC samples implanted at 850°C and annealed at 1200°C demonstrated n-type electrical behaviour. P-type behaviour was only observed when the sample was annealed at 1400°C. Similarly, measurements in [24] demonstrated an activation level for the dopants of less than 1%. Such inefficient holes' generation process demands high acceptor dopant concentration for p-type 3C-SiC which in turn induces more lattice defects deteriorating the hole mobility. This challenge can be a limiting factor for conventional 3C-SiC-on-Si MOSFET designs.

In this paper, a novel process flow is proposed for the fabrication of vertical 3C-SiC-on-Si MOSFETs which eliminates the need for Al implantation. This includes a homo-epitaxially grown p-layer on top of the n-drift layer, rather than formatting the p-body with multiple implants. The proposed design has been developed with the Technology Computer Aided Design (TCAD) Synopsys Process tool and its performance simulated with Synopsys Device tool. A previously validated set of physics models are used to accurately describe the 3C-SiC material which was previously published in [25], [26]. Traps at the interface between SiO_2/3C-SiC have also been included with density values that agree with reported fabricated structures in the literature for this technology. The results in this work highlight that the proposed design is able to deliver 3C-SiC-on-Si MOSFETs with excellent output characteristics.

II. The Conventional MOSFET Design Method

The simulated conventional design of the 3C-SiC MOSFET follows the common rules for any similar planar power FET. The n-type $5x10^{15}cm^{-3}$ drift layer is considered to be 10μm thick and grown by hetero-epitaxy on an isotype Si substrate. The substrate is assumed to be 350μm thick and $1x10^{19}cm^{-3}$ doped. The doping of the implanted p-body regions is $1x10^{18}cm^{-3}$, whilst the source n+ regions are highly doped to ensure good ohmic contacts. The gate oxide is 60nm. The active area of the device considered for this work is $7.3x10^{-4}$ cm^2 and it is equivalent to the fabricated 3C-SiC MOSFET in [14]. Moreover, fixed charges are considered at the SiO_2/3C-SiC interface with a value of $4.5x10^{12}$ cm^{-2} [5], [17].

A. SRIM simulations for 3C-SiC

The p-body region plays a key role in the performance of the conventional MOSFET design, therefore, accurate Monte Carlo simulations were performed to investigate the trends of the Aluminium (Al) implant in the 3C-SiC. For this purpose, the 3C-SiC target material was modelled in SRIM/TRIM software [27]. The compound target feature stoichiometry close to 1:1 after accurate measurements of the Si/C ratio [28], a density value of 3.166 g/cm^3 [29] and threshold displacement energies of 20eV for Carbon (C) and 35eV for Si [30]. This study adopted surface binding energies of 7.4eV and 4.7eV for C and Si respectively [31].

Notably, two major TRIM limitations must be interpreted: (a) There is no build-up of ions or damage in the target. Every ion is calculated with the assumption of zero dose. This indicates that the target is considered perfect and previous ions have no effect on subsequent ions. (b) The target temperature is 0K, and there are no thermal effects changing the distribution of ions (thermal diffusion) or affecting the target damage (thermal annealing). The latter is less significant, as the diffusion of dopants in SiC is negligible.

The resulting simulations in SRIM highlighted a known issue of the implantation process. In particular, for depths very close to the surface of the semiconductor there are difficulties in achieving the desired concentration of dopants. For this purpose, implantations with oxide cap were also considered. Effectively, this shifts the peak of the

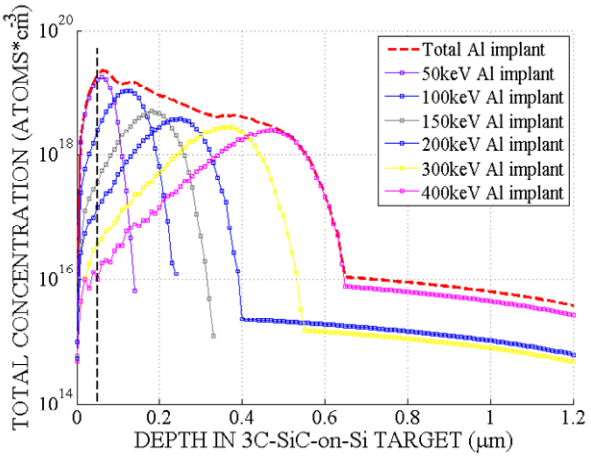

Fig. 1. The combination of the chosen Al implants for a 3C-SiC target material to create a gradual decreasing net doping profile for the p-body regions. The peak concentration of $1x10^{18}cm^{-3}$ is at the channel region.

resulted distribution closer to the surface after the cap layer is removed. Further, the removal of this sacrificial oxide layer also removes 0.05μm up to 0.1μm of the semiconductor. This in turn, ensures that the new surface of the semiconductor will be within the peak of a Gaussian distribution for a specific implantation energy and a specific dopant type. The implantations targeted to form the p-body region in the 3C-SiC with an activated Al concentration of approximately $1x10^{18}$ cm^{-3}. The total implanted doping profile to serve this purpose is illustrated in Fig. 1 and consists of 6 consecutive implants.

B. Process simulations and Performance Evaluation

Complete cells are considered for simulations in this work, for more accurate results. In contrast to the half-cell case, this configuration includes the interaction between adjacent cells. Further, for the simulation purposes, the body and source terminals are connected to the same node.

The process steps for the fabrication of the conventional 3C-SiC-on-Si MOSFET design are illustrated in Fig. 2. The sProcess tool has been utilized in TCAD Sentaurus software [32] to accurately model all these required steps. To facilitate the removal of 0.05μm from the 3C-SiC surface due to the sacrificial oxide, an additional etching step has been included in the process.

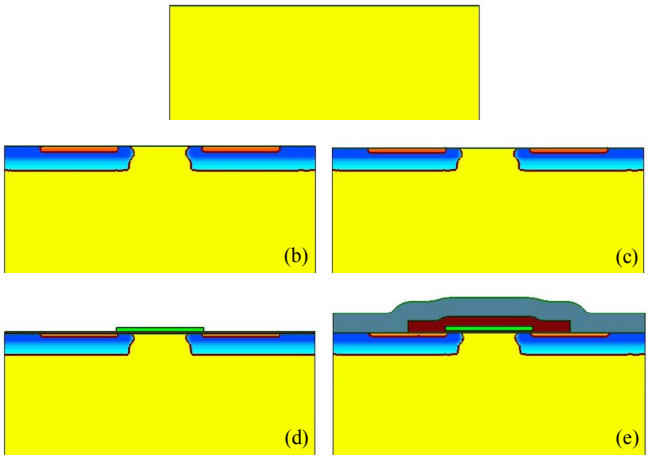

Fig. 2. The process of a conventional design of a 3C-SiC-on-Si MOSFET in steps: (a) heteroepitaxy of the 3C-SiC drift layer on Si substrate, (b) implantation of the implants shown in Fig. 1 and thereafter implantation to form the source region, (c) 0.05μm are etched from the surface of the semiconductor to ensure that the channel region will be sufficiently doped, (d) gate oxide growth and deposition of poly-Si for the gate contact, (e) metallization.

TABLE I: SIMULATED OUTPUT CHARACTERISTIC VALUES FOR THE DESIGN IN FIG. 1 ASSUMING $4.5X10^{12}$ CM^{-2} OXIDE/3C-SIC INTERFACIAL TRAPS.

	Gate Threshold Voltage	***On-Resistance***	***Breakdown Voltage at avalanche onset***
Conventional Design	4.964 Volts	91.5 Ohm	720 Volts

The on-state and the forward breakdown simulations were also performed with TCAD software by utilizing an accurate and validated material model for the 3C-SiC [21]. Table I briefly summarizes the simulated characteristic values for the conventional design of a 3C-SiC-on-Si MOSFET. The on-resistance has been calculated as the slope of the simulated I_D-V_D plot, for V_D=0.5Volts and V_G=10Volts. These values have been selected to ensure that all the 3C-SiC-on-Si MOSFETs discussed in this paper operate in the linear region.

III. THE PROPOSED 3C-SIC-ON-SI MOSFET DESIGN

The viability of the conventional design method is under question for 3C-SiC-on-Si MOSFETs because of the reported challenges in the activation of p-type dopants in the cubic SiC polytype. In an effort to address this major material-related issue, an alternative MOSFET design is proposed in this paper.

Instead of forming the p-body regions by implantation, it is proposed to grow a thin 3C-SiC layer of p-type conductivity on top of the hetero-epitaxially grown n-drift 3C-SiC layer. This can be achieved by changing the SiC epitaxial film growth conditions in the chamber from N to Al rich environment. Thereafter, the JFET region can be shaped with implants of N in the desired areas, given that no issues have been reported regarding the activation of N in 3C-SiC-on-Si in the literature.

A. The implanted JFET region in 3C-SiC-on-Si

The SRIM simulator was utilized, similarly to Section II, to investigate the ranges of the N in the 3C-SiC target. Several implants with varying implantation energies were simulated to obtain the distributions of the N dopants and the achieved penetration depth. Thereafter, the best combination of these distributions was selected to form a quasi-constant doping profile. The doses were calculated upon the fluence of each implant after the requirement for a doping concentration slightly above the p-body layer one.

However, this particular task proves to be quite challenging due to the high concentration difference between the p-body layer and the n-drift layer. The implants should be precisely controlled in order to compensate the body layer dopants and reverse the conductivity type for the formation of the JFET region. On the other hand, the resulting JFET doping should have a value as close as possible to the n-drift layer concentration.

The total implanted doping profile to form the JFET region in the p-3C-SiC layer is illustrated in Fig. 3. This profile was incorporated into the process tool to simulate the fabrication of this MOSFET design. The resulting structure is shown in steps in Fig. 4. The characterization process revealed very good on-state characteristics, similar to the conventional design reported in Section II. On the contrary, very poor blocking capabilities and an excessive leakage

current were demonstrated. The results are briefly presented in Table II.

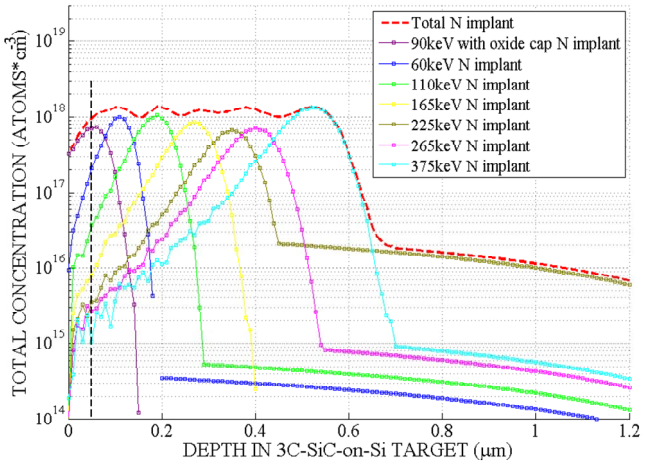

Fig. 3. The combination of the chosen N implants for a 3C-SiC target material to create a quasi-constant net doping profile for the implanted JFET region. The desired minimum concentration for this purpose is approximately $1.01x10^{18}cm^{-3}$ in order to successfully compensate the highly doped p-body epitaxially grown 3C-SiC layer.

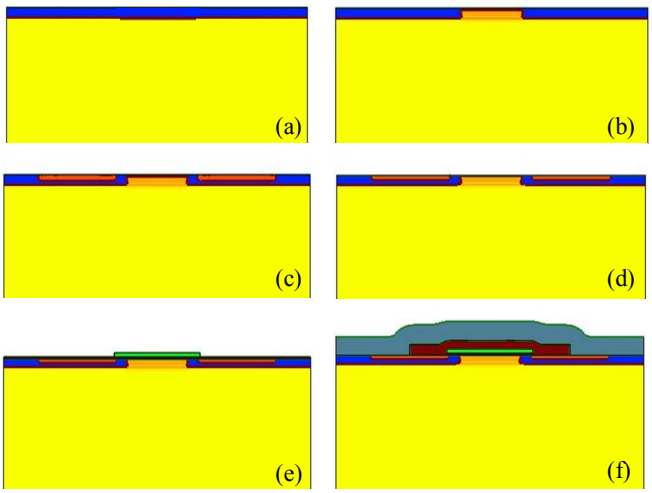

Fig. 4. The process of the proposed design of a 3C-SiC-on-Si MOSFET in steps: (a) heteroepitaxy of the 3C-SiC drift layer on Si substrate and on top of that homoepitaxy of the p-type 3C-SiC body layer, (b) implantation of the implants shown in Fig. 3 for the formation of the JFET region, (c) implantation for the formation of the source regions, (d) 0.05μm are etched from the surface of the semiconductor to ensure that the channel region will be sufficiently doped, (e) gate oxide growth and deposition of poly-Si for the gate contact, (f) metallization.

The uniformly and highly doped p-body epi-layer of 3C-SiC, is difficult to be precisely compensated by multiple N implantations in order to form the JFET region. In addition, the number of implants should not exceed a maximum value if both the lattice damage and the total cost of the device should be kept low. Thus, trying to compensate the $1x10^{18}$ cm^{-3}, even small variations above this value can cause the formed JFET region to have areas with a resulting doping of orders of magnitude greater compared to the n-drift layer. This can effectively deteriorate the blocking capabilities of the device.

TABLE II: SIMULATED OUTPUT CHARACTERISTIC VALUES FOR THE DESIGN IN FIG. 4 ASSUMING $4.5X10^{12}$ CM^{-2} OXIDE/3C-SIC INTERFACIAL TRAPS.

		Gate Threshold Voltage	*On-Resistance*	*Breakdown Voltage at avalanche onset*
Implanted JFET Design	Uniformly doped p-body	1.326 Volts	8.6 Ohm	-
	Thin p-body layers of variable doping	4.875 Volts	12.8 Ohm	111 Volts

To improve the forward blocking characteristics, the process for the epitaxy of the p-body layer was modified. By varying the parameters of the epitaxy environment, the doping profile of the resulted p-type 3C-SiC can be engineered. Thus, a more gradual doping profile was selected for this layer, rather than the uniform one considered initially. Particularly, the p-type 3C-SiC layer splits in sub-layers epitaxially grown on top of each other with controllable doping concentration. In consequence, the sub-layer that includes the channel region features the desired peak concentration of activated Al dopants. Towards the n-drift 3C-SiC layer, the Al concentration of the following sub-layers gradually decreases.

This can be beneficial for the suggested design process of the MOSFET. In fact, considering the uniformly doped epitaxially grown p-body layer and the implantation profile in Fig. 3, the residual doping can be more than an order of magnitude larger than the drift doping value. This is highlighted by the deep yellow areas in the formed JFET region in Fig. 4. Splitting the p-body region in thin sub-layers enables for a more effective compensation by adjusting the doses of each of the implant steps. In turn a smoother doping profile can be obtained in the JFET with values closer to the drift layer N concentration. This has a direct impact on the performance of the device; an increased blocking capability and a reduced electric field in the JFET region are now observed.

Taking into account this design variation, as shown in Table II, the forward blocking is improved. Nonetheless, the suggested design still fails to meet the blocking voltage expectations compared to the conventional design.

IV. OPTIMIZATION OF THE PROPOSED 3C-SIC-ON-SI MOSFET DESIGN

To further improve the forward breakdown performance of the power device the distance between the two adjacent p-body regimes should be decreased. The process steps for such a suggested optimization are illustrated in Fig. 5. By comparing the Fig. 4 with Fig. 5, the effect of having

consecutive thin p-type layers, to form the p-body layer by epitaxy, can be observed. To improve the forward breakdown performance, the lower parts of the p-body regions are extended towards the JFET [33]. This concurrently brings closer the two p-body regions and preserves a JFET region under the gate contact of lower resistant. The simulated output characteristics of this optimized design are briefly presented in Table III.

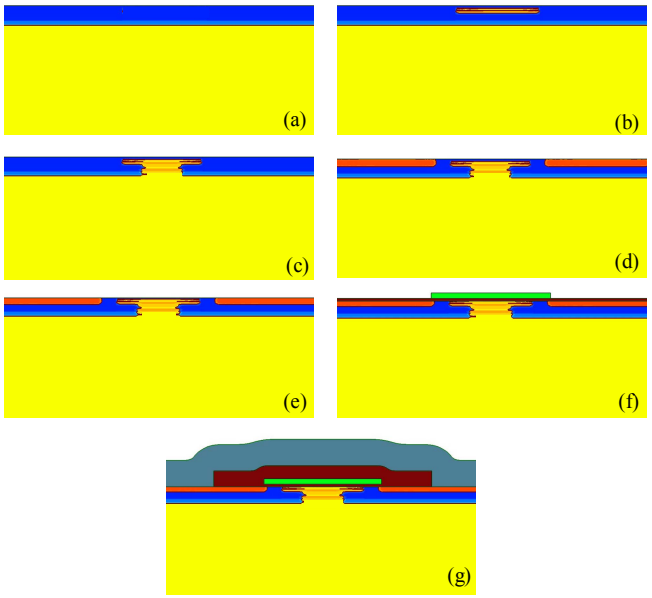

Fig. 5. The process of the proposed design after optimization for a 3C-SiC-on-Si MOSFET in steps: (a) heteroepitaxy of the 3C-SiC drift layer on Si substrate and on top of that homoepitaxy of the p-type 3C-SiC body layer, (b) implantation of the implants up to the energy of 225keV as shown in Fig. 3 for the formation of the first part of the JFET region, (c) an additional mask is utilized to perform the rest higher energy implants with a spatial limitation to form the extended p-body edges [33], (d) implantation for the formation of the source regions, (e) 0.05μm are etched from the surface of the semiconductor to ensure that the channel region will be sufficiently doped, (f) gate oxide growth and deposition of poly-Si for the gate contact, (g) metallization.

TABLE III: SIMULATED OUTPUT CHARACTERISTIC VALUES FOR THE DESIGN IN FIG. 5 ASSUMING $4.5\text{x}10^{12}$ CM^{-2} OXIDE/3C-SIC INTERFACIAL TRAPS.

	Gate Threshold Voltage	***On-Resistance***	***Breakdown Voltage at avalanche onset***
Optimized Design	4.78 Volts	15.9 Ohm	570 Volts

V. RESULTS AND DISCUSSION

In this paper a novel process flow for the fabrication of vertical 3C-SiC-on-Si n-MOSFETs has been proposed in order to resolve material related issues. Instead of utilizing ion implantation to form the p-body region, a thin layer of p-type conductivity can be grown by homo-epitaxy. Thereafter, the JFET region can be created by N implants which over compensate the p-type layer. In this section the output characteristics of the simulated proposed design with and without the p-body extension region (optimized design) are compared with the ones of the conventional MOSFET design method.

Fig. 6 depicts the transfer characteristics. As shown, the gate threshold voltage is similar for all cases, which ensures that the devices can be compared directly. The gate oxide thickness is kept the same, with a value of 60nm. The same stands for the SiO_2/3C-SiC-on-Si traps with a value of $4.5\text{x}10^{12}$ cm^{-2}.

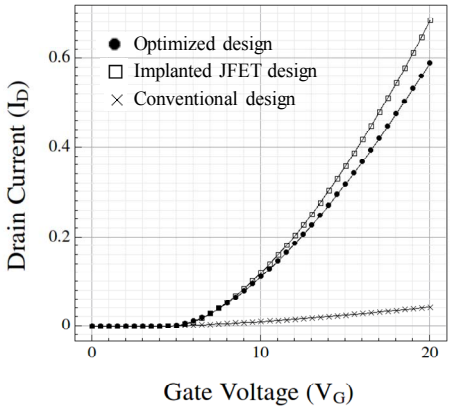

Fig. 6. Transfer Characteristics. The threshold voltage of the three investigated designs is similar whilst the on-resistance is drastically reduced for the proposed designs.

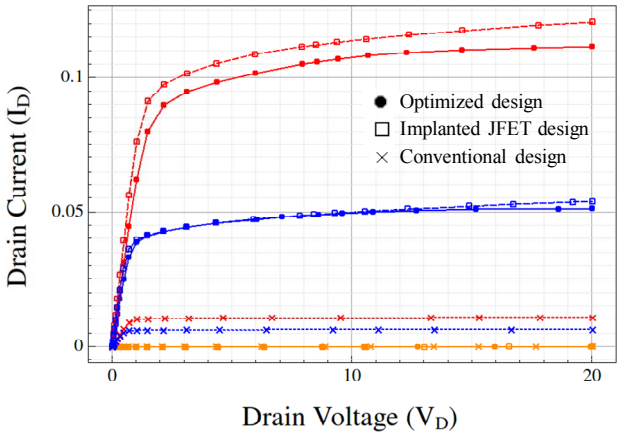

Fig. 7. Simulated output characteristics of the investigated $7.3\text{x}10^{4}$ cm^{-2} 3C-SiC-on-Si MOSFET designs. The red colour corresponds to V_G=10V, the blue to V_G=8V and the orange to V_G=4V.

The simulated I_D-V_D plot in Fig. 7 is drawn for gate voltages of 4V, 8V and 10V. With the conventional design method, the JFET region is one of the major contributors to the total MOSFET resistance. It is observed that the proposed designs have lower on-resistance compared to the conventional one, which is attributed to the much higher doping concentration of the JFET region. The consequence of having a highly doped JFET is a reduction in the blocking ability. This is illustrated in Fig. 8. The optimized proposed design method features extended p-body edges towards the JFET region, as described in a previous section. This enables for a better distribution of the electrostatic potential in the JFET and n-drift layer, resulting in a forward

breakdown value directly comparable with the one obtained from the conventional design method. Indeed, the blocking ability achieved is over 600V.

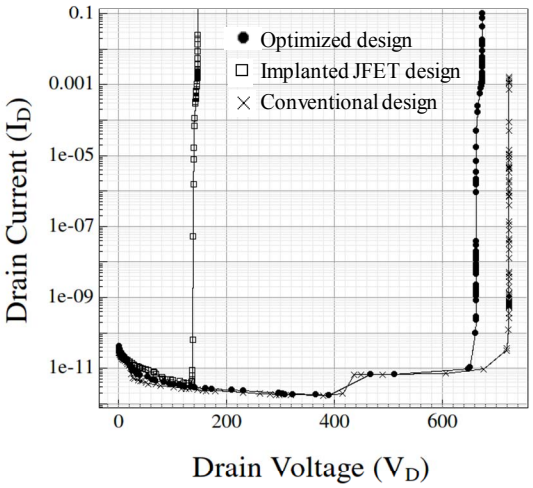

Fig. 8. The proposed design method simulated output characteristics suggest that a forward breakdown voltage can be supported with a value similar to the one featured by the conventional design method. Unless optimized, the forward breakdown characteristics are majorly deteriorated.

VI. Conclusions

Summarizing, the novel proposed design moethod, investigated in this paper, has the premises to deliver viable 3C-SiC-on-Si MOSFETs by resolving some well-known material related limitations. Thereafter, based on this work, the authors target to perform a physics-based simulation robustness analysis, including a comparison of the short circuit capability of the proposed design to the conventional.

References

[1] A. A. Lebedev, S. P. Lebedev, V. Y. Davydov, S. N. Novikov, and Y. N. Makarov, "Growth and investigation SiC based heterostructures," in *15th Biennial Baltic Electronics Conference (BEC)*, 2016, pp. 5–6.

[2] T. Tachibana, H. S. Kong, Y. C. Wang, and R. F. Davis, "Hall measurements as a function of temperature on monocrystalline SiC thin films," *J. Appl. Phys.*, vol. 67, no. 6375, 1990.

[3] H. Nagasawa, K. Yagi, T. Kawahara, and N. Hatta, "Properties of Free-Standing 3C-SiC Monocrystals grown on Undulant- Si (001) Substrate," vol. 436, pp. 3–8, 2003.

[4] H. Nagasawa *et al.*, "Low-Defect 3C-SiC Grown on Undulant-Si (001) Substrates," in *Silicon Carbide Recent Major Advances*, W. J. Choyke, H. Matsunami, and G. Pensl, Eds. Berlin: Springer, 2004.

[5] B. A. Schöner, M. Krieger, G. Pensl, M. Abe, and H. Nagasawa, "Fabrication and Characterization of 3C-SiC-Based MOSFETs," pp. 523–530, 2006.

[6] B. Van Zeghbroeck and H. Fardi, "Comparison of 3C-SiC and 4H-SiC Power MOSFETs," vol. 924, pp. 774–777, 2018.

[7] M. Bakowski, "Status and Prospects of SiC Power Devices Status and Prospects of SiC Power Devices," *IEEJ Trans. Ind. Appl.*, vol. 126, no. 4, pp. 391–399, 2006.

[8] M. Krieger, G. Pensl, M. Bakowski, and A. Schöner, "Hall Effect in the Channel of 3C-SiC MOSFETs," *Mater. Sci. Forum*, vol. 485, pp. 441–444, 2005.

[9] J. Wan, M. A. Capano, M. R. Melloch, and J. A. Cooper, "N-channel 3C-SiC MOSFETs on silicon substrate," *IEEE Electron Device Lett.*, vol. 23, no. 8, pp. 482–484, 2002.

[10] T. O. Hshima *et al.*, "The Electrical Characteristics of Metal-Oxide-Semiconductor Field Effect Transistors Fabricated on Cubic Silicon Carbide," *Jpn. J. Appl. Phys.*, vol. 42, 2003.

[11] K. K. Lee *et al.*, "N-Channel MOSFETs Fabricated on Homoepitaxy-Grown 3C-SiC Films," *IEEE Electron Device Lett.*, vol. 24, no. 7, pp. 466–468, 2003.

[12] A. Schöner *et al.*, "Realisation of Large Area 3C-SiC MOSFETs," *Mater. Sci. Forum*, vol. 483–485, pp. 801–804, 2005.

[13] M. Abe *et al.*, "High current capability of 3C-SiC vertical DMOSFETs," *Microelectron. Eng.*, vol. 83, no. 1 SPEC. ISS., pp. 24–26, 2006.

[14] M. Bakowski *et al.*, "Development of 3C-SiC MOSFETs," *J. Telecommun. Inf. Technol.*, pp. 49–56, 2007.

[15] H. Search, C. Journals, A. Contact, M. Iopscience, and I. P. Address, "High-Temperature Operation of Silicon Carbide MOSFET," vol. 310.

[16] E. Sakuma, H. Daimon, and M. Yamanaka, "Experimental 3C-Sic MOSFET," vol. 1, no. 7, pp. 404–406, 1986.

[17] H. Nagasawa, M. Abe, K. Yagi, T. Kawahara, and N. Hatta, "Fabrication of high performance 3C□SiC vertical MOSFETs by reducing planar defects," *Phys. status solidi*, vol. 1280, no. 7, pp. 1272–1280, 2008.

[18] H. Nagasawa, K. Yagi, T. Kawahara, N. Hatta, and M. Abe, "Hetero- and homo-epitaxial growth of 3C-SiC for MOS-FETs," *Microelectron. Eng.*, vol. 83, pp. 185–188, 2006.

[19] H. Search, C. Journals, A. Contact, M. Iopscience, and I. P. Address, "Band alignment and defect states at SiC / oxide," vol. 1839.

[20] F. Ciobanu, G. Pensl, V. Afanas, and A. Schöner, "Low Density of Interface States in n-type 4H-SiC MOS Capacitors Achieved by Nitrogen Implantation," *Mater. Sci. Forum*, vol. 485, pp. 693–696, 2005.

[21] A. Arvanitopoulos, N. Lophitis, K. N. Gyftakis, S. Perkins, and M. Antoniou, "Validated physical models and parameters of bulk 3C-SiC aiming for credible technology computer aided design (TCAD) simulation," *Semicond. Sci. Technol.*, vol. 32, no. 10, p. 104009, 2017.

[22] T. Kimoto, K. Kawahara, and H. Niwa, "Ion implantation technology in SiC for power device applications," *Junction Technol. (...*, no. V, pp. 4–9, 2014.

[23] M. V. Rao *et al.*, "Al and B ion-implantations in 6H- and 3C-SiC," *J. Appl. Phys.*, vol. 77, no. 6, pp. 2479–2485, 1995.

[24] L. Wang *et al.*, "Demonstration of p-type 3CSiC grown on 150 mm Si(1 0 0) substrates by atomic-layer epitaxy at 1000 °c," *J. Cryst. Growth*, vol. 329, no. 1, pp. 67–70, 2011.

[25] A. Arvanitopoulos, N. Lophitis, K. N. Gyftakis, S. Perkins, and M. Antoniou, "Validated physical models and parameters of bulk 3C-SiC aiming for credible Technology Computer Aided Design (TCAD) simulation," *IOP Semicond. Sci. Technol.*, vol. 32, no. 10, p. 104009, Oct. 2017.

[26] N. Lophitis, A. Arvanitopoulos, S. Perkins, and M. Antoniou, "TCAD Device Modelling and Simulation of Wide Bandgap Power Semiconductors," in *Disruptive Wide Bandgap Semiconductors, Related Technologies, and Their Applications*, Y. K. Sharma, Ed. Rijeka: InTech, 2018.

[27] J. F. Ziegler, "SRIM/TRIM code." .

[28] M. Roumie, M. Tabbal, B. Nsouli, and A. Said, "Determination of stoichiometry in silicon carbide materials using elastic backscattering spectrometry," *Nucl. Instrum. Methods B*, vol. 260, pp. 637–641, 2007.

[29] "Silicon Carbide." [Online]. Available: http://www.ioffe.ru/SVA/NSM/Semicond/SiC. [Accessed: 01-Jan-2017].

[30] W. Jiang *et al.*, "Progress in Characterization of Precipitates and Defect Structures in Mg+ Ion Implanted Cubic Silicon Carbide," in *Fusion Reactor Materials Program Semiannual Progress Reports*, F. W. Wiffen, R. Godfrey, and B. Waddel, Eds. 2015.

[31] J. Chang, J. Cho, C. Gil, and W. Lee, "A simple method to calculate the displacement damage cross section of silicon carbide," *Nucl. Eng. Technol.*, vol. 46, no. 4, 2014.

[32] Synopsys, "Sentaurus TM Structure Process User Guide.," 2017.

[33] P. Ward, N. Lophitis, T. Trajkovic, and F. Udrea, "High voltage semiconductor devices," US 20170243937, Aug-2017.

AUTHORS' INFORMATION

Arvanitopoulos E. Anastasios was born in Patras, Greece, in May 1985. He received the Diploma in Electrical and Computer Engineering from the University of Patras, Greece in 2011. Since October of 2016 he has been a Ph.D. Candidate at the Research Institute for Future Transport and Cities, Coventry University, UK. His research is focused on Wide Bandgap (WBG) power semiconductor devices for high performance electronics in Electric Vehicles (EVs). Of his particular interest is the physical modelling of WBG semiconductor materials and devices aiming to accurately simulate the effect of defects in the device operation.

Marina Antoniou received the B.A. and M. Eng. degrees in electrical and information engineering from the University of Cambridge (Trinity College), Cambridge, U.K., and the Ph.D. degree in electrical engineering from Cambridge. She was a Junior Research Fellow in Selwyn College, Cambridge, U.K. She is currently an Associate Professor at the University of Warwick and is also affiliated with the U.K. Power Electronics Centre. Her research interests include power electronics and high voltage power semiconductor devices.

Fan Li received the B.Eng. degree in mechanical engineering from the University of Birmingham in 2011 and M.Sc. degree in engineering from the Cranfield University in 2012. From 2012 to 2016, he studied as a Ph. D student in University of Warwick in the area of WBG semiconductor power devices. Since then, he worked as a research fellow in the same institution. His research interests include design, fabrication and characterising of power devices on novel materials, such as 3C-SiC, Si on SiC, Ga_2O_3, etc.

Mike Jennings received his BEng degree in Electronics with Communications from the University of Wales, Swansea, UK in 2003. The BEng incorporated a second year (exchange program) of study in the USA, where he studied at Union College, Schenectady, NY. His interest in semiconductor device modelling, processing and characterisation led him to undertake a PhD, in the field of silicon carbide (SiC) power electronics at the University of Warwick, UK. During his PhD he has won travel scholarships from the IEE (Hudswell Bequest Fellowship) and Welsh Livery Guild for electrical engineering research purposes. The scholarships obtained allowed him to visit Rensselaer Polytechnic Institute, NY, USA in 2005. He successfully defended his PhD, entitled "Novel Contact Formation for 4H-SiC Power Devices" in 2008. In 2009 Mike was awarded a Science City Research Alliance (SCRA) Fellowship, sponsored by the European Regional Development Fund (ERDF) and Advantage West Midlands (AWM). The focus of his research within this remit was the "Development of SiC Devices". His current research topics include high voltage bipolar devices (PiN diodes and Thyristors) in SiC, novel gate oxidation processes for Field Effect Transistors (FET) and 3C-SiC (cubic) growth above direct wafer bonded Si/SiC structures. Mike continues to work on the above topics as an active member of the Systems and Process Engineering Centre within the College of Engineering, Swansea University. He is a lecturer on numerous electrical engineering courses including IC design and power semiconductor devices.

Samuel Perkins was born in Norwich in the United Kingdom, on September 17th, 1993. He received his B.Eng. and MRes degrees from Coventry University, Coventry, in 2017. Currently he is pursuing his PhD degree at Coventry University. His research is focused on Wide Bandgap (WBG) power semiconductor devices for Ultra High Voltage applications. Of his particular interest is the physical modelling of WBG semiconductor materials and characterisation of 4H-SiC n-IGBTs for Ultra High Voltage applications.

Konstantinos N. Gyftakis (M'11) was born in Patras, Greece, in May 1984. He received the Diploma in Electrical and Computer Engineering from the University of Patras, Patras, Greece in 2010. He pursued a Ph.D in the same institution in the area of electrical machines condition monitoring and fault diagnosis (2010-2014). Then he worked as a Post-Doctoral Research Assistant in the Dept. of Engineering Science, University of Oxford, UK (2014-2015). Then he worked as Lecturer (2015-2018) and Senior Lecturer (2018-2019) in the School of Computing, Electronics and Mathematics and as an Associate with the Research Institute for Future Transport and Cities, Coventry University, UK. Additionally, since 2016 he has been a member of the "Centro de Investigação em Sistemas Electromecatrónicos" (CISE), Portugal. Since 2019 he has been a Lecturer in Electrical Machines, University of Edinburgh, UK. He has authored/co-authored more than 70 papers in international scientific journals and conferences and a chapter for the book: "Diagnosis and Fault Tolerance of Electrical Machines, Power Electronics and Drives", IET, 2018.

Neophytos Lophitis received the B.A. and M.Eng. degrees in 2009 and the Ph.D. degree in Power Devices in 2014, all from the University of Cambridge. Then he worked as a Research Associate in Power at the University of Cambridge (2014-15) and as a consultant for Power Microelectronics companies (2013-15). He joined Coventry University in 2015 where he is currently an Assistant Professor of Electrical Engineering at the School of Computing, Electronics & Mathematics and the research Institute for Future Transport and Cities. Since 2015 he has also been a member of the "High Voltage Microelectronics Laboratory" at the University of Cambridge, UK. Neophytos is also affiliated with the U.K. Power Electronics Centre and the European Centre for Power Electronics. His research includes optimization, design, degradation and reliability of high voltage microelectronic devices and electrical energy storage and conversion systems. He authored/co-authored more than 45 scientific manuscripts, including one book chapter for the book: "Disruptive Wide Bandgap Semiconductors, Related Technologies, and Their Applications", IntechOpen, 2018.