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Performance and reliability of commercial GaN-on-Si power devices

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Performance and Reliability of Commercial GaN-on-Si Power Devices

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ABSTRACT

Commercial GaN-on-Si based power devices are now available up to the 650 V class. Theoretically GaN-on-Si power devices offer extremely high performance capabilities and relatively low production costs. The unique material properties of GaN have attracted a lot of attention from the power electronic sector within the past 20 years. The combination of high thermal conductivity, critical electric field, wide bandgap, high electron saturation and the plateau of traditional Silicon technology has motivated this interest. However, the development of commercial GaN-on-Si device has been shrouded in complex and extensive challenges. Normally-on operation, current collapse and high levels of crystal defects are to name but a few. Furthermore, Silicon Super-junction technology has recently seen rapid progression in their performance and production costs. This has indirectly slowed the adoption of GaN-on-Si power devices.

The direction of GaN-on-Si based power HEMT devices is split among manufactures. Panasonic, GaNsystems and EPC have adopted GaN-on-Si GIT Enhancement mode devices. Whereas; Transphorm has pioneered the cascode GaN-on-Si HEMT. Both GaN-on-Si technologies have been developed for similar voltage and current classes. As the technologies are significantly different it is logical to assume that the performance of these devices will be.

In this thesis, naturally Enhancement mode and cascode GaN-on-GIT enhancement mode GaN-on-Si power devices are characterised in terms of their static characteristics at room temperature and at their maximum rated temperatures. The experimental result of this characterisation shows the immense difference between the different behaviour of the two different GaN-on-Si power devices. Therefore, systems designers need to consider the differences before device choice.

ACKNOWLEDGEMENTS

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LIST OF ABBREVIATIONS AND ACRONYMS

2DEG	Two Dimensional Electron Gas
AlGaN	Aluminium Gallium Nitride
AlN	Aluminium Nitride
C-V	Capacitance Voltage
D-mode	Depletion mode
DUT	Device Under Test
E-mode	Enhancement mode
Fl	Fluorine
GaAs	Gallium Arsenide
GaN	Gallium Nitride
HEMT	High Electron Mobility Transistor
HFET	High Fields Effect Transistor
HTRB	High Temperature Reverse Bias
HV	High Voltage
HVOS	High Voltage Off State
InN	Indium Nitride
LV	Low Voltage
MISFET	Metal Insulated Semiconductor Field Effect Transistor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MOVCD	Metal Organic Vapour Chemical Deposition
Si	Silicon
SiC	Silicon Carbide
SJ	Super Junction
Si_3N_4	Silicon Nitride
WBG	Wide Band Gap

LIST OF SYMBOLS

A	Area	m^2
C	Capacitance	F
E_C	Conduction band energy	eV
E_F	Fermi level energy	eV
E_g	Band gap energy	eV
E_V	Valance band energy	eV
G_M	Transconductance	mS/mm
I_{DS}	Drain to Source Current	A
L_{GD}	Gate to drain length	m
L_{GS}	Gate to source length	m
L_{SD}	Source to drain length	m
P_{PE}	Piezoelectric polarization	C/m^2
P_{SP}	Spontaneous polarization	C/m^2
R_{CH}	Resistance of the channel	Ω
R_{DS}	Drain to source resistance	Ω
R_{ON}	On resistance	$\Omega.mm^2$
V_{BR}	Breakdown voltage	V
V_{GS}	Gate to source voltage	V
V_{TH}	Threshold voltage	V
Tox	Gate oxide thickness	m
W_g	Gate width	m
v_{sat}	Saturation electron velocity	m/s^{-1}
μ_e	Electron Mobility	$cm^2/V.s$

1 INTRODUCTION

P   *ower electronics is essential for efficient and economic management of electrical power. At the heart of*
 power electronics is the power device. The field of power devices has exponentially grown since its conception in the early 1940's. New device topologies, packaging improvements and the introduction of Wide Band Gap (WBG) materials have expanded the field of Power Electronics significantly. This chapter explores the fundamentals of power electronics, power semiconductors, conventional power devices and the industrial requirements for modern power devices. In addition, this chapter details the rise of WBG power semiconductors and briefly discusses their development, focusing specifically on the Gallium Nitride (GaN) material. Finally, at the end of this chapter an outline for the rest of this thesis is presented.

1.1 Fundamental Concepts of Power Electronics

Power electronics is the practice of efficient electrical power management through the use of solid state power devices [1]. Electrical power management broadly encompasses the process of control and conversion of electrical power. Control emphasises the significance of information over energy and conversion emphasises the significance of energy over information. These principles are illustrated in figure 1.1.
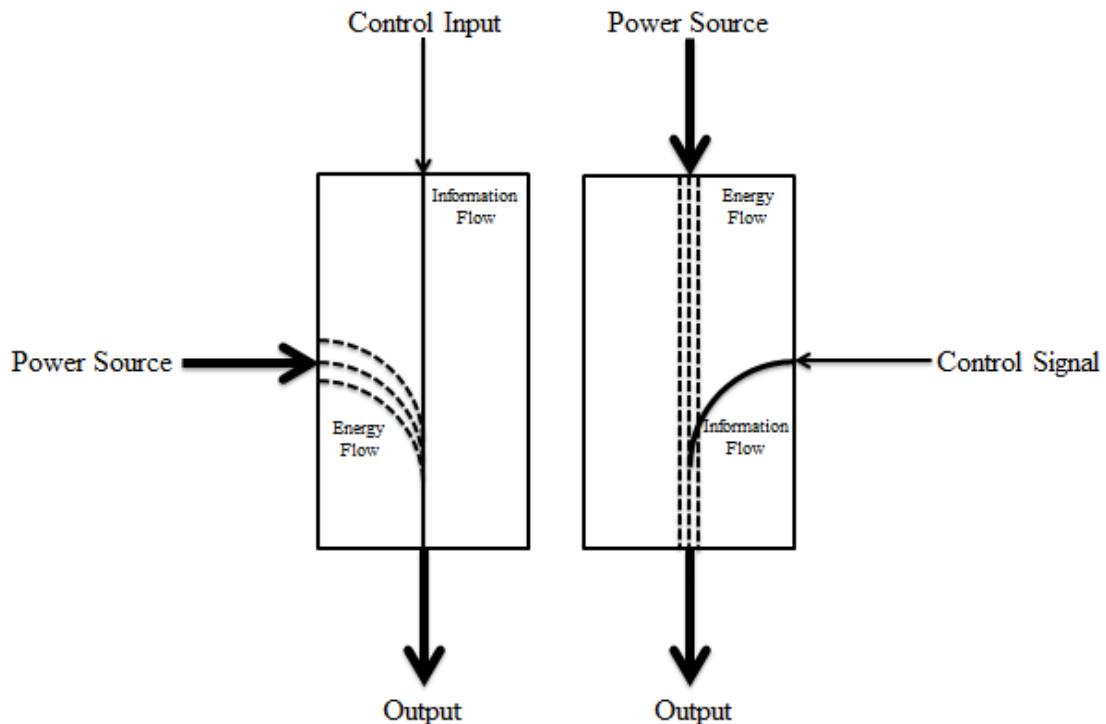
Fig 1-1Block diagram of the electrical control and conversion principles redrawn from [2]

1.1.1 A Brief Introduction to the Power Device

Before the more complex principles of power devices are discussed, it is important to clarify and introduce power devices as a whole. Power devices are composed of a semiconducting material. A semiconductor's identity lies in its material properties i.e. the relative distance between the Fermi level and the conduction band [3]. The Fermi level is the greatest or highest state occupied by carriers (electrons) at absolute zero [4]. An illustration of the concept of material classification can be seen in figure 1.2.
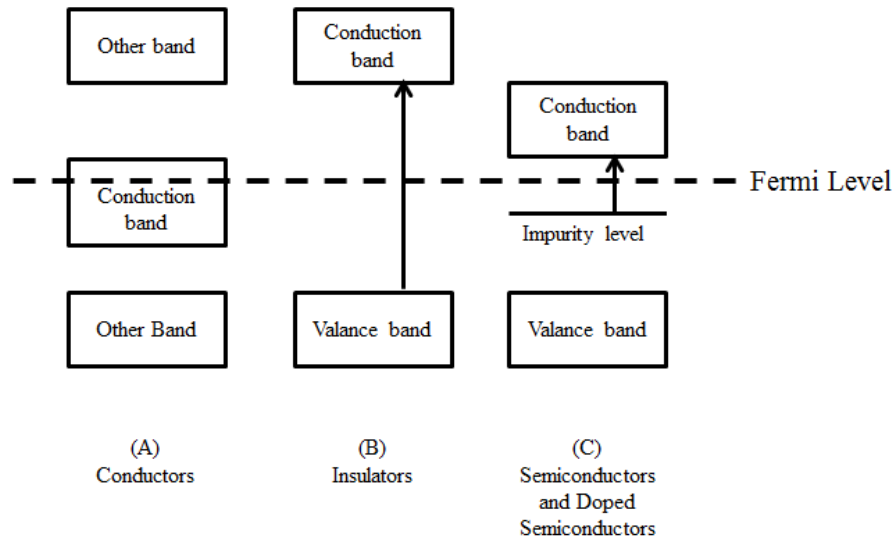
Fig 1-2 The relative position of the Fermi level in relation to the conduction band of typical conductors, insulators and semiconductors redrawn from [5]

Materials conduct electricity when charge carriers exist in the conduction band. Depicted in figure 1.2 the Fermi level of conductors overlaps into the conduction band. Conductors, therefore, have charge carriers in the conduction band and exhibit good electrical conductivity, although, it should be stated that if the conduction band is full of carriers the material will display poor electrical conductivity. The Fermi level within insulators is a relativity large distance away from the conduction band and thus can be thought to have poor electrical conductivity. Semiconductors on the other hand, display tendencies of both conductors and insulators. Their Fermi level is a relatively small distance away from the conduction band and therefore, can be easily manipulated through doping to achieve resistive or conductive behaviour. The distinction between insulators and semiconductors is particularly unclear, however, semiconductors in general can be characterised by the following properties;

- Semiconductors have poor electrical resistivity and poor conductivity.
- As the temperature increases the semiconductor's electrical resistivity decreases.
- A semiconductor's electrical resistivity is an intermediate value that can be manipulated.
- Generally a semiconductor's electrical resistivity lies between 10^{-2} to 10^6 Ω.cm and does not behave in ohmic fashion.
- Generally a semiconductor's band gap energy is in the region of 0 to 4 *eV*. Although, this is not always true as in the case of diamond and various other semiconductors.
- A semiconductor is susceptible to visible light.
- A semiconductor displays strong thermoelectric effects.

[6] [7] [8] [9]

The actual power device is an arrangement of semiconductors in a structure, in which, the individual semiconductors (layers) interact. The concept of power devices will be discussed in greater detail through this thesis. The purpose of this work however, will be investigating and exploring Gallium Nitride based power devices and therefore, traditional Silicon technology will not be discussed in great detail.

1.1.2 The Role of Power Devices

The solid-state power devices mentioned in the initial introduction statement in the context of this thesis refer to power semiconductor devices i.e. Silicon Controlled Rectifiers (SCR), p-n diodes, thyristors, Metal Oxide Semiconductor Field Effect Transistors (MOSFETs), Insulated-gate Bipolar Transistors (IGBTs), High Electron Mobility Transistors (HEMTs) etc. These devices are discussed in the coming subchapters however, out of these devices the HEMT device will be the only device discussed in depth. Power semiconductor devices are commonly employed as switches. One such example of a solid-state power device utilized as power switch is the DC/DC buck converter illustrated in figure 1.3.
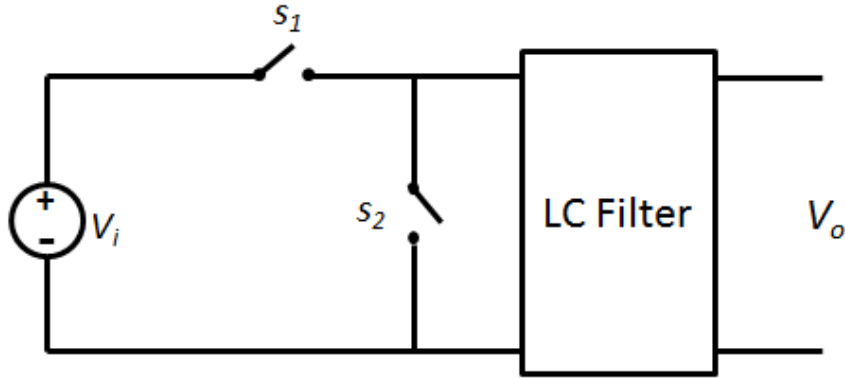
Fig 1-3 An example of a simple DC/DC buck converter employing power switches S_1 and S_2, adapted from [10]
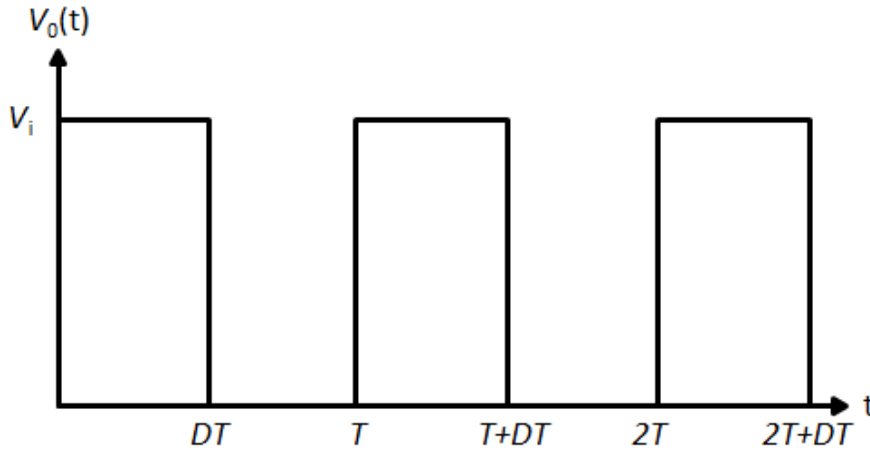
Fig 1-4 The waveforms of the simple DC/DC buck converter

The use of power devices as switches has provided a significant improvement of efficiency compared to other forms of converters such as systems that use linear electronics. In the DC/DC buck converter displayed in figure 1.3 the output voltage of the circuit is equal to the input voltage when switch 1 is on. Conversely, when switch 2 is on the output voltage for the circuit is equal to 0. The duty cycle (D) of the system is the ratio of the on time of switch 1 compared to the period T. Therefore, as the output voltage of this circuit is an intermittent signal the LC filter is used to achieve a DC voltage. The output voltage for this system can be represented mathematically by;

$$V_{out,av} = \frac{1}{T} \int_0^{DT} V_i = DV_i$$

(Eq.1.1)

As most cases dictate the D < 1. The average DC output voltage is subsequently always less than the input voltage supplied to the circuit. This circuit is, therefore, referred to as a step down or buck converter. This is a relatively simple circuit; however, the principle of power switches being used is extremely important. It should be noted that this example assumes the ideal operation of the power switches in the circuit. In the next subchapter the ideal properties of power switches are discussed and so are the real-world properties.

1.2 The Ideal Properties of Power Switches

As previously discussed power devices are commonly referred to as power switches due to their operating requirements. The development of such power switches has introduced new topologies, structures, materials and packaging to provide superior switching characteristics; therefore, the accurate and precise ideal characteristics for power switches must be stated, so that device development is progressive. The classification of the ideal power switch is similar to that of a mechanical switch [1]. These four ideal principles can be stated as the switch possessing [11] [12] [13];

- Zero bidirectional current conduction in the off-state.
- Zero bidirectional voltage exertion in the on-state.
- Zero transient period between the on and off-state.
- Infinite current and voltage capabilities.

Furthermore, considering commercial power switches the development must acknowledge several more significant properties.

- Zero device degradation.
- Minimal controlled switching energy.
- Minimal size, weight and cost.
- Operationally robust in different environments.
- Zero electromagnetic radiation interference.

Applying the assumption described above, power switches can be generally classified into three control categories.

1. The uncontrollable switch, this has no internal control mechanism.

2. The semi-controllable switch, this has minimal internal control of the operation of the switch.

3. The fully controllable switch, this device can be completely controlled through a control terminal.

[1]

Although obvious, these statements are necessary for the efficient development of the power switch. The ideal principles give engineers an ultimate objective and when industrial power devices are discussed their performance will ultimately be compared to the statements above. Actual power devices, however, do not behave ideally and are restricted through material and physical limitations. Regarding the power loss of switches three common examples of losses include; the on state, off state and the transient losses. In the on state the power switch has a voltage drop across it. In the off state the device exhibits leakage current. During the transient period between the on and off state there is time and therefore, power loss. The power device losses will be dissipated as thermal energy and therefore, will raise the temperature of the switch causing further complications. These characteristics prevent 100% efficiency of the power devices. More practical constraints such as AC dispersion or as it is more commonly referred to current collapse will be focused on later due to the size and depth of the topic. The discussion will be focused on GaN devices but many of these principles will be similar for most power semiconductors.
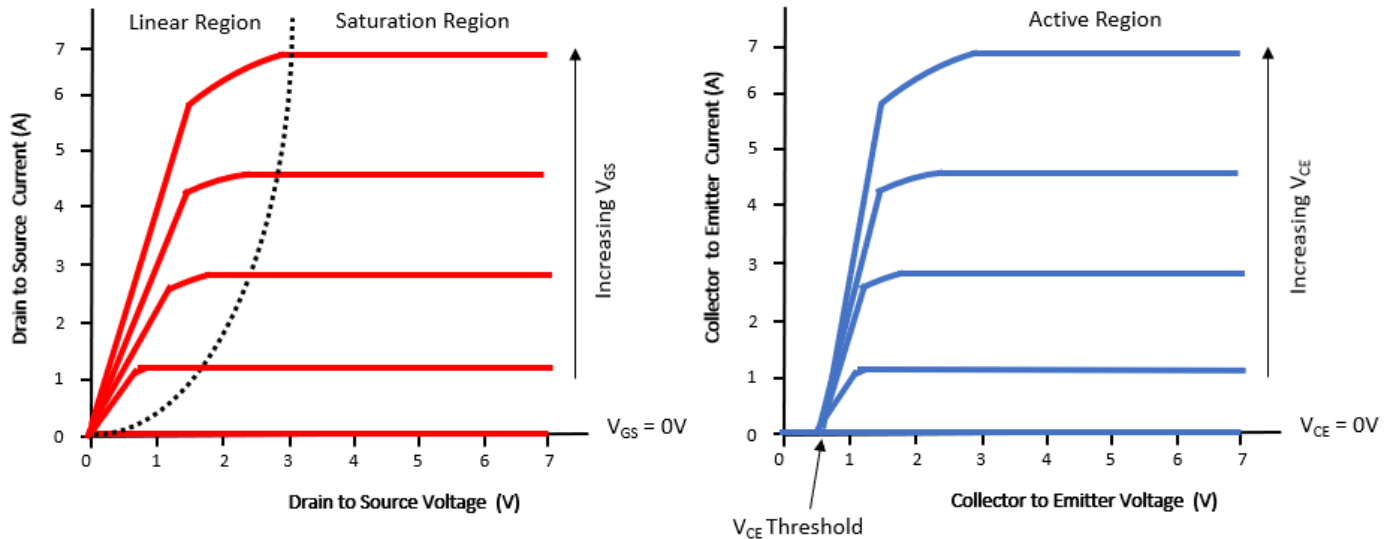
Fig 1-5 Ideal I-V characteristics of a MOSFET (left) and IGBT (right) power devices

1.3 Requirements for Industrial Power Applications

The field of industrial power applications is extensive and incorporates a large spectrum of operational requirements from High Voltage Direct Current (HVDC) applications to refrigeration [14]. Figure 1.6 illustrates a few examples of the typical industrial applications that power devices are required for. This graph also details a simplified representation of the power and frequency requirements.
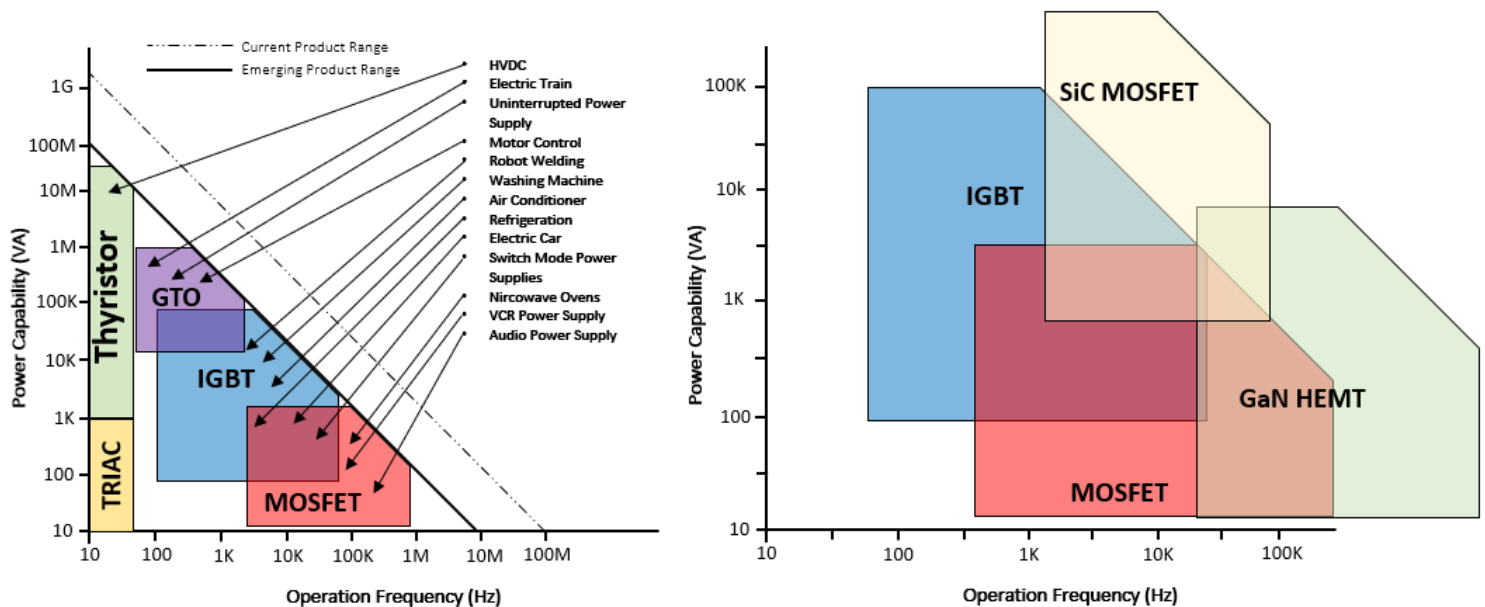
Fig 1-6 (left) Application requirements of Si power electronic devices (right) the introduction of new device technologies GaN HEMTs and SiC MOSFETs adapted from [15]

From figure 1.6 it is clear that devices are used for systems that require different operating conditions such as power and frequency. Towards the higher power capacity spectrum of this graph HVDC systems are required to handle many megawatts of power and operate at low frequencies. In the middle section of this graph Electric Vehicles (EV) chargers and inverters are required to handle moderate power and moderate frequencies. Finally,

at the opposite end of the spectrum, there is relatively high frequency requirements for DC to DC and AC to DC converters as well as Power Factor Correction (PFC) circuits which are used extensively in power supplies.

In general, as the power capacity requirements increase the operating frequency requirements reduce. Traditionally thyristors are employed in HVDC applications because of the devices low on state resistance. IGBTs are favoured for the medium frequency and medium power applications such as household electrics and MOSFETs are favoured for the high frequency, lower power applications. However, there are many overlaps between these devices.

1.4 The Development of Commercial Power Devices

The field and types of solid state power devices grew rapidly after the introduction of the SCR in 1957 [10]. In this section a brief overall of notable developments of power device is discussed.
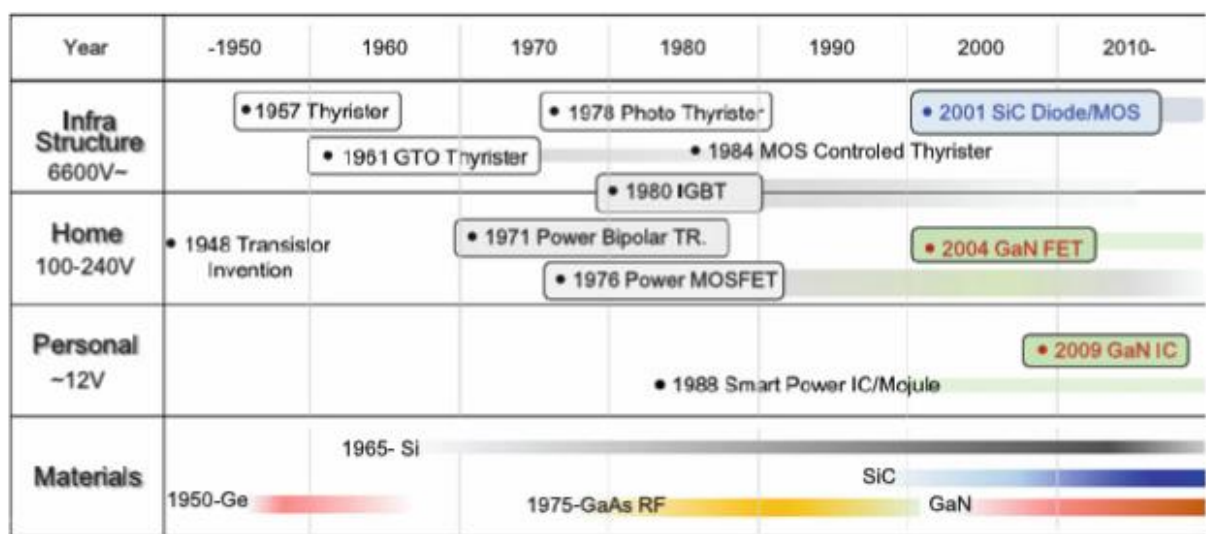
Fig 1-7 The development of power devices throughout history [16]

Briefly discussing the devices in figure 1.7 the Bipolar Junction Transistor (BJT) was invented in 1948. The BJT was used in applications that require moderate power and frequency. However, this device has become obsolete in the main stream applications. The gate turn-off thyristor (GTO) was introduced in 1961 and is used in applications from medium to high power and from low to medium frequencies. The MOSFET was developed in 1970 [17] and is used for low to moderate power applications which require high frequencies. The IGBT was developed in 1980 [18] and is used in applications from low to medium power and frequency. The integrated gate commutated thyristor (IGCT) invented in 1997 [19] is used in applications from medium to high power and from low to medium frequencies. In 2001 the first 4H-SiC Schottky diode was commercially introduced, marking a significant milestone for WBG power devices. The GaN FET was introduced in 2004 and is fast becoming attractive for applications that the Silicon (Si) MOSFET previously dominated.

1.5 The Introduction of Wide Band Gap Power Devices

WBG power devices have recently been commercialised and are now directly competing with their Si counterparts. Traditional Silicon technology has dominated the field of power electronics since the 1960's and it should be noted that it continues to do so, as market sales prove. However, the material limits for conventional Si technology advancements in terms of efficiency, size, weight, robustness and general all-round performance is beginning to plateau at their theoretical limits.
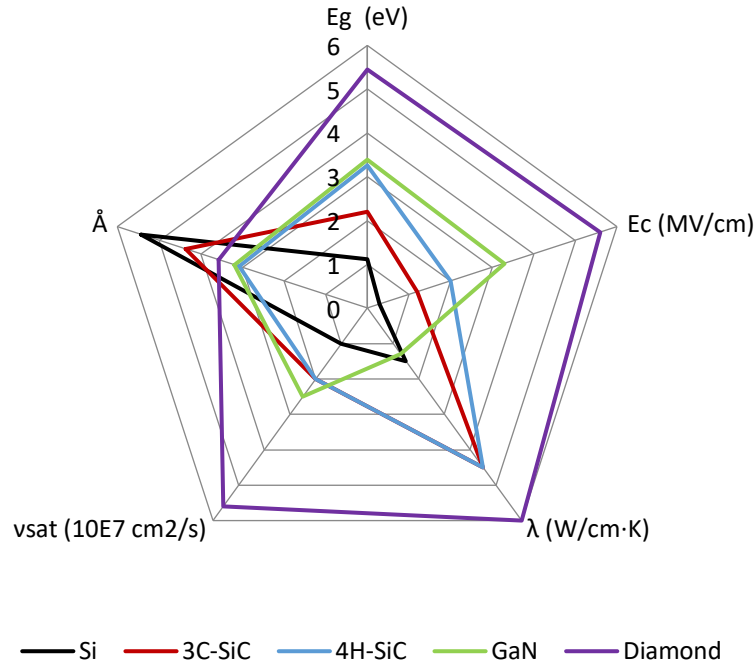
Fig 1-8 Material properties of significant power semiconductors normalised against Si, data taken form [16] and [20]

Parameter	Si	3C-SiC	4H-SiC	GaN	Diamond
Band Gap Energy (eV)	1.12	2.2	3.26	3.39	5.45
Critical Electric Field Strength (MV/cm)	0.3	1.2	2	3.3	5.6
Thermal Conductivity (W/cm.K)	1.5	4.5	4.5	1.3	6
Saturation velocity ($x10^7 cm^2/s$)	1	2	2	2.5	5.6
Lattice Constant (Å)	5.43095	4.359	3.073	3.189	3.567

Tab 1 Material properties of significant power semiconductors against Si, data from Fig 1-8

Figure 1.8 displays significant properties of power semiconductors, where E_g represents the band gap energy, E_c the critical electric field strength, λ the thermal conductivity, v_{sat} the carrier saturation velocity and $Å$ the crystal lattice constant. $Å$ has primarily been included because this is very important for economic reasons. WBG materials are expensive and it is far more complex to grow native substrates, so WBG semiconductors with a $Å$ close to Silicon's is desirable. This concept will be discussed in far greater detail later.

WBG materials possess many superior properties over Silicon; this makes them potentially more suitable for certain applications including high speed, high temperature and high efficiency systems. WBG materials have larger band gaps than Silicon. The materials' band gap energy is the difference between the valance and conduction band. In an intrinsic semiconductor carriers are forbidden to occupy this region [21]. Therefore, larger band gaps require more energy to promote carriers from the valence band into the conduction band. This is extremely important for high temperature environments. This is primarily down to the electron phonon interaction for temperatures above 100K and the change in bond lengths [22]. GaN has a band gap energy of 3.39 *eV*. 4H-SiC has a band gap energy of 3.26 *eV* and Si has a band gap energy of 1.12 *eV*. Having a large band gap energy ensures a low intrinsic carrier concentration n_i, as the amount of energy required to promote electrons increases. This is very important for the characteristics of leakage current and WBG materials should display at least a leakage current several of orders lower than that of Silicon's. Low intrinsic carrier concentration ultimately allows high efficiencies and offers the capability for high temperature operation.
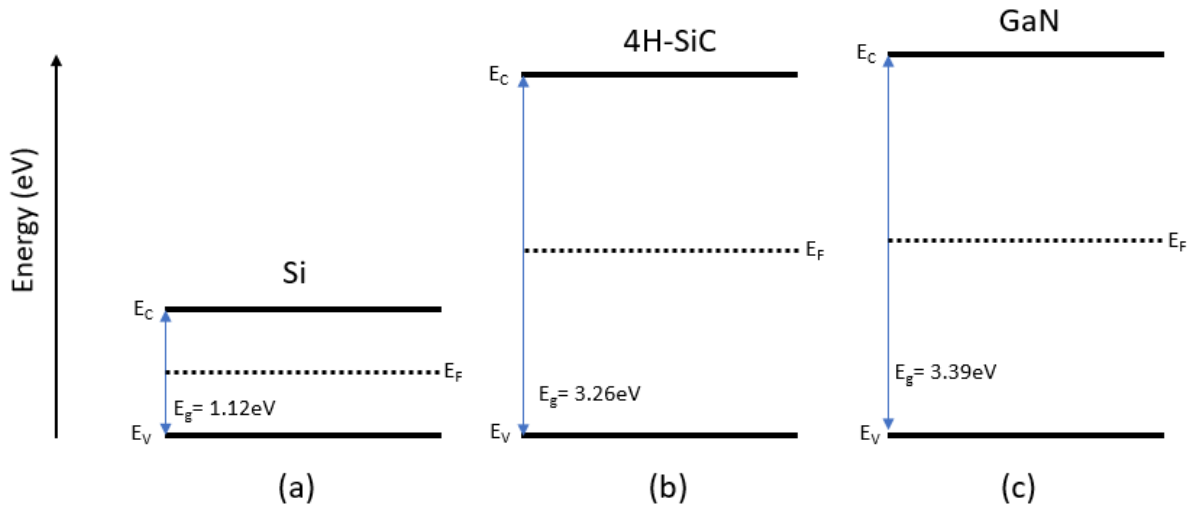
Fig 1-9 The energy band gap for Si (a), 4H-SiC (b) and GaN (c)

Also, it is clear from figure 1.8 WBG materials display superior electric breakdown field strengths over Silicon. The electric breakdown field strength is the minimum voltage per unit of area usually *cm* that causes the material to become electrically conductive at will. Materials with higher electric breakdown field strengths will have higher breakdown voltages. This is extremely important in high power applications [23]. This property has a strong influence on the size of the depletion area [24]. This allows the design of thinner drift layers for given blocking voltages, therefore the yield for R_{ON} is drastically reduced and furthermore, minimises the device size, leading to smaller device capacitances and therefore switching losses are reduced. This allows higher switching frequencies and in turn reduces the switching losses.

The saturation velocity is the maximum velocity of a charge carrier when an electric field that is greater than the materials critical value is applied. This is because of phonon emission and ultimately results in reduced response times for devices [25]. High saturation velocity is therefore desired for fast and efficient switching performances. Higher switching performances also allow the reduction in size of passive components such as capacitors and inductors, which take up a considerable size in the system, see figure 1.10.
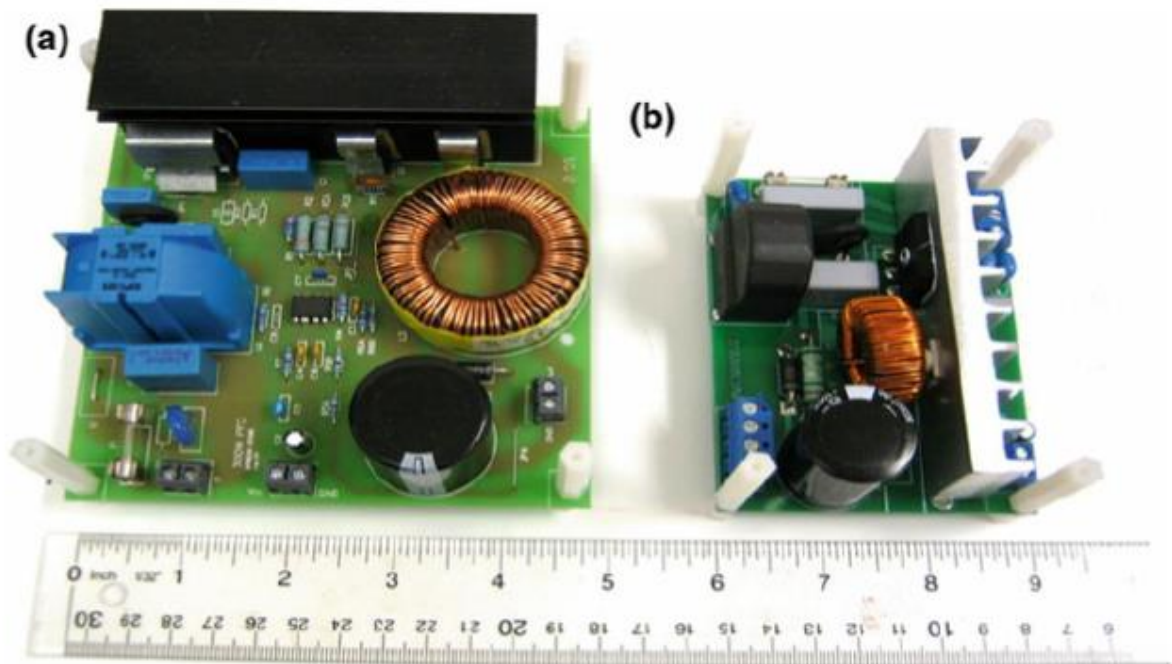
Fig 1-10 The reduction of size in a PFC circuit (a) PFC circuit utilizing Silicon technology and (b) PFC circuit utilizing GaN technology [26]

The property of thermal conductivity has recently become more significant in the field of power electronics. The thermal conductivity of a material is its ability to conduct heat. It is important for devices to have high thermal conductivity as it means that heat is conducted away faster and therefore, devices can be used in environments of higher temperatures without complex cooling systems [27]. The polytypes of SiC and Diamond materials are far superior in this respect, although it should be stated that packaging limitation may prevent the full advantages of this property. GaN displays a thermal conductivity marginally inferior to that of Silicon.

Another interesting property of a material is their dielectric constant. The dielectric constant is the ratio between the material's permittivity compared to that of a vacuum's. By having a low dielectric constant the parasitic capacitances are reduced, making the device's switching speed faster [28]. This is especially important for high speed operations in the *MHz* range.

Considering the superior characteristics that WBG materials offer over Silicon it is easy to see why we are seeing the integration of WBG power devices into the market. Although, it must be stated this is only one route for the development of advanced power switches Si Super Junctions have shown remarkable progress up to date and even have slowed down WBG device adoption. In addition, the development of reliable GaN power devices has been thwarted in complex difficulties such as growth and AC dispersion issues but these will be discussed in later chapters.

1.5.1 The Impact of WBG Power Devices for the R_{ON} and BV Relationship

Power devices are designed to achieve high blocking capabilities and low on state resistances, in order to meet the needs of industrial applications. The equation for the specific on resistance for vertical power devices is mathematically represented by;

$$R_{ON} = \frac{4BV^2}{\varepsilon_s \, \mu_n \, E_c^3}$$

[29]

(Eq.1.2)

Where; the denominator $\varepsilon_s \, \mu_n \, E_c^3$ of this equation is referred to as Baliga's figure of merit for power devices. The assumption of the drift region resistance with the electron mobility is made because of the probability of electrons having far greater mobility values. Conversely, the equation for the specific on resistance (R_{ON}) for lateral power devices is mathematically represented by;

$$R_{ON} = \frac{BV^2}{q \, \mu_n \, n_s \, E_c^2}$$

[29]

(Eq.1.3)

The use of these formulas has enabled direct comparison between different device topologies as shown in figure 1.11. Therefore, GaN power devices offer the potential for superior R_{ON} – BV characteristics for conventional device design.
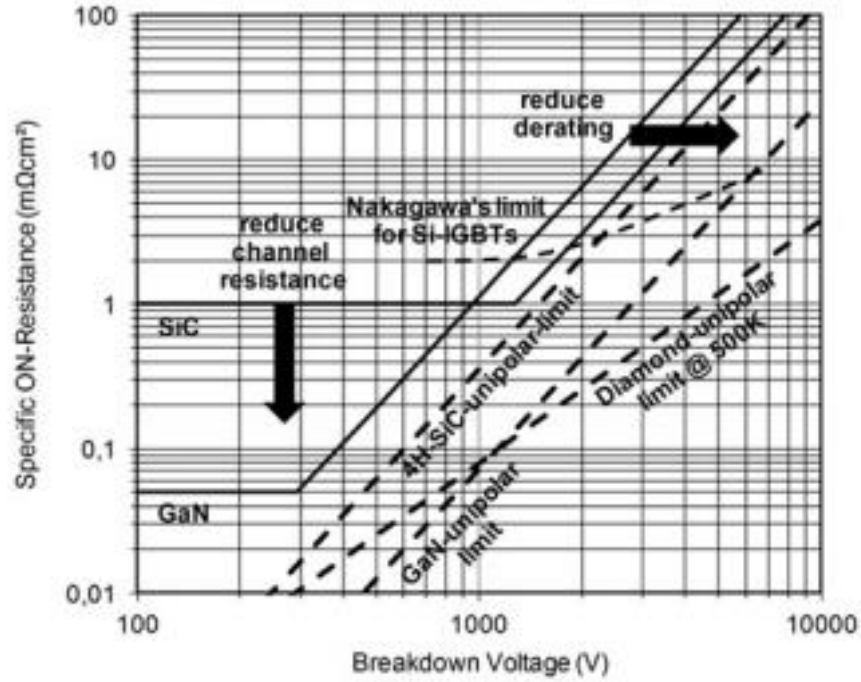
Fig 1-11 R_{ON} vs BV for unipolar devices with different types of materials [30]

1.5.2 Determination of WBG Semiconductor Performances through FOMs

Figure of Merits (FOMs) have been used to compare and rate different semiconductors. There have been many FOMS developed to determine the performance of semiconductors across a spectrum of conditions. The Johnson's limit (FOM) is used to describe the trade-off between the BV and high frequency operation. This is dependent on the material properties in the power device and is mathematically described as;

$$JFOM = BV \cdot f_T = \frac{E_c \cdot v_{sat}}{2\pi}$$

(Eq.1.4)

[16]

Baliga's Figure of Merit (BFOM) was developed for determining the performance of semiconductors in conditions of low frequency, thus conduction is the prominent form of power losses.

$$BFOM = \varepsilon_s \, \mu_n \, E_c^3$$

(Eq.1.5)

[29]

Baliga developed the High Frequency Figure of Merit (BHFOM) for determining the performance of semiconductors in conditions of high frequency, thus switching frequencies are the prominent form of power losses.

$$BHFOM = \mu \, E_c^2$$

(Eq.1.6)

[29]

More specialised FOMs have been developed. The Keyes FOM includes thermal limitations.

$$KFOM = \theta_k \cdot \sqrt{\left(\frac{c\, v_{sat}}{4\pi\varepsilon_r}\right)}$$

[31]

(Eq.1.7)

Another more specialised FOM is the Combined FOM (CFOM) this considers high power, frequency and temperature conditions.

$$CFOM = \theta_k \cdot \varepsilon_r . \mu \cdot v_{sat} E_c^2$$

[32]

(Eq.1.8)

Although, it should be stated that FOM's are not an exact science as they are developed for particular traits such as temperature, speed and on-state characteristics. This therefore, means they should be only used as an indication rather than performance conformation. Table 2 displays the FOMs for unipolar devices normalised against Silicon for the GaN, 4H-SiC 3C-SiC and Diamond semiconductor materials.

Semiconductor	JFOM	BFOM	BHFOM	KFOM
Si	1	1	1	1
3C-SiC	65	33.4	10.3	1.6
4H-SiC	180	130	22.9	4.61
GaN	760	650	77.8	1.6
Diamond	2540	4110	470	32.1

Tab 2 FOMs for WBG unipolar devices normalised against Silicon data collected from [33] and [34] see appendix.

1.5.3 Future Prospects for WBG Power Devices

Referring back to figure 1.6 the full and successful integration of SiC and GaN power devices will significantly change the maximum capabilities and distribution of devices on the market. One such example of the theoretical power industrial application graph is depicted in figure 1.12.
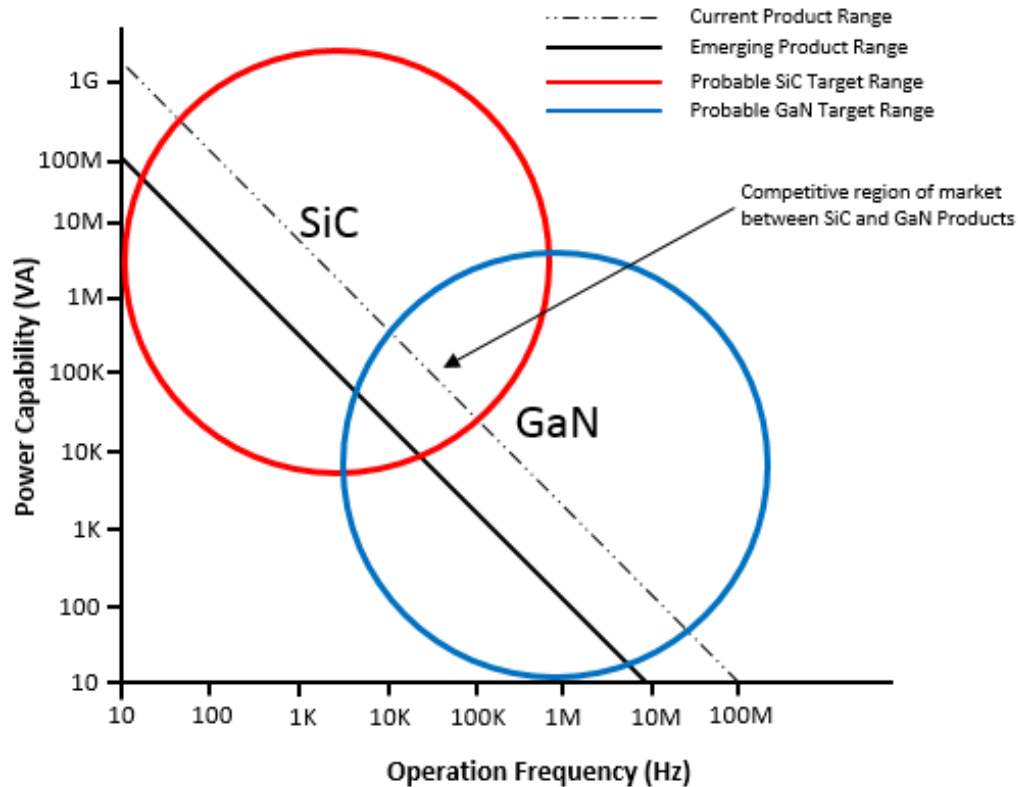
Fig 1-12 Introduction of WBG power devices into the industrial power market adapted from [35] *and Fig 1.6*

WBG semiconductors have already demonstrated remarkable performances and have already been introduced into the power device market. GaN based power devices have already been proven to be reliable and efficient with impressive blocking voltages. That being said, GaN remains far behind its' theoretical limits and further understanding and development is needed. This statement is strengthened by the current range of GaN based devices available. These devices are incredibly different in nature and both are being marketed for similarly rated classes.

1.5.4 Important Milestones for GaN Power Devices
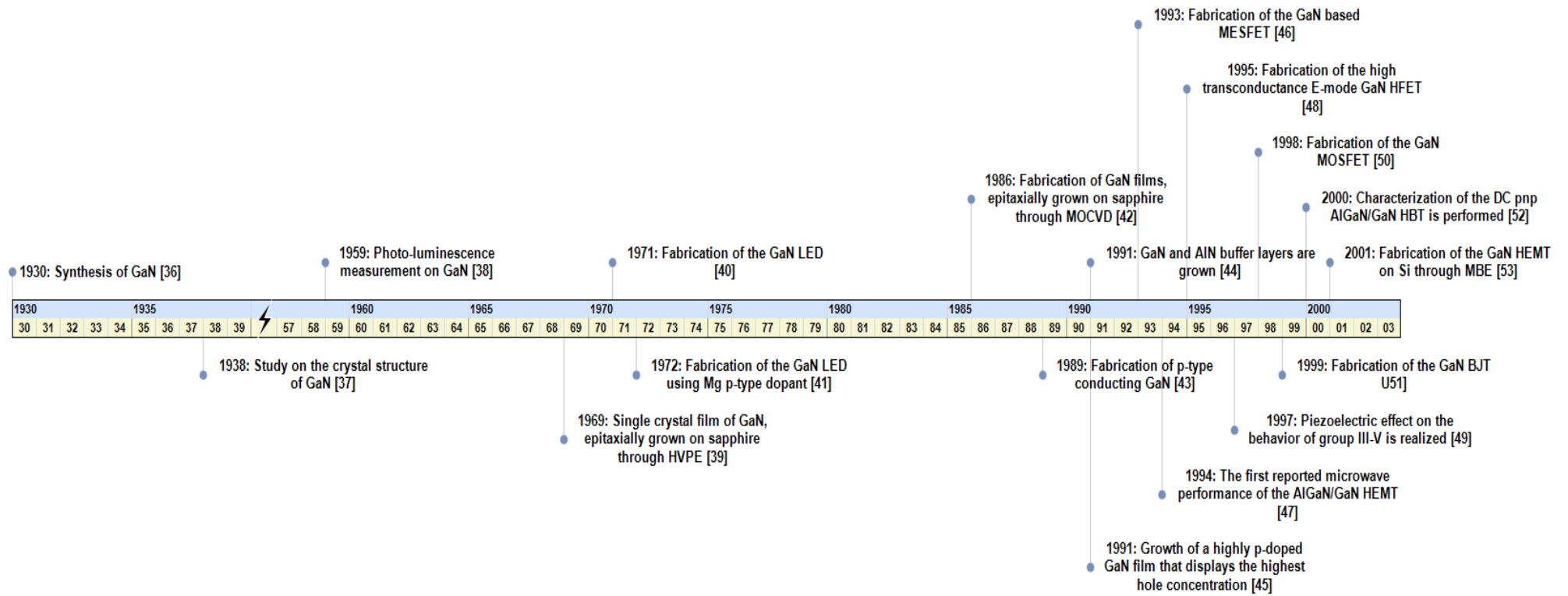
Fig 1-13 Important Milestones for GaN Power Devices Before 2001

[36], [37], [38], [39], [40], [41], [42], [43], [44], [45], [46], [47], [48], [49], [50], [51], [52], [53]
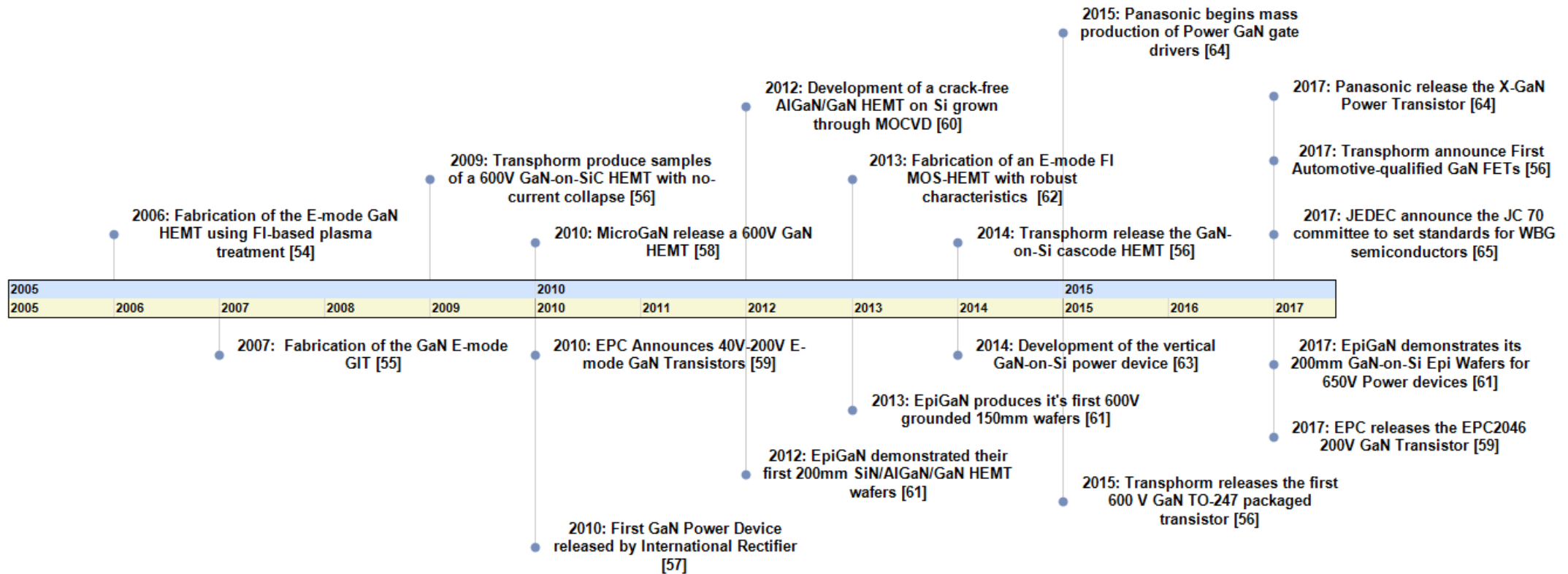
Fig 1-14 Important Milestones for GaN Power Devices Post 2001

[54], [55], [56], [57], [58], [59], [60], [61], [62], [63], [64], [65].

1.6 Research Aims and Objectives

The main focus of this thesis is the accurate characterisation and analysis of commercial GaN-on-Si power devices. As previously mentioned, manufacturers have developed commercial GaN-on-Si power devices through different designs aiming for the same voltage class. In addition, the rapid progression of Si super junction technology has provided high performance power devices at a fractions cost and it is widely accepted that they have limited the growth of WBG power devices. Specifically, this work aims to provide the following data;

1. Static characterisation at 300 K of similarly rated, Cascode GaN-on-Si HEMT, E-mode GaN GIT and Si super junction power devices.
2. Elevated static characterisation at > 300 K of similarly rated Cascode GaN-on-Si HEMT, E-mode GaN GIT and Si super junction power devices.
3. Reliability data of similarly rated Cascode GaN-on-Si HEMT, E-mode GaN GIT and Si super junction power devices.

The data provided through experimentation will be used to comprehensibly analyse the development of GaN-on-Si technology. In addition, the inclusion of Si super junction technology will indicate the performance of the two different GaN-on-Si device technologies to a relative standard.

1.7 Outline of This Thesis

Chapter 2 presents the fundamental theory behind GaN HEMT based devices. The individual material properties of AlGaN and GaN are explored and the subsequent formation of the 2DEG channel from the AlGaN/GaN interface is presented. Ga and N face crystal lattices are illustrated, and their properties are analysed. Following this, the operation of the basic GaN HEMT is discussed with the aid of illustrations and a detailed band diagram is developed. In addition, a basic technique for the growth of GaN HEMTs is discussed. Finally, this chapter discusses commercial GaN-on-Si focusing on the Transphorm cascode device and the Panasonic GIT. A summary is presented at the end of this chapter.

A detailed methodology and evaluation of the static performance of state-of –the-art commercial GaN-on-Si devices using the B1505A Power Device Analyzer is documented in **Chapter 3**. A brief etiquette to accurate measurements using the B1505A is discussed along with the experimental setup. Forward I-V, reverse I-V, Transfer characteristics, R_{ON}, C-V measurements and break down voltage measurements are presented. In addition, recent commercialised Si super junctions are introduced to provide reference to the performance of the GaN-on-Si devices.

Finally, in **Chapter 5** this works' conclusions are presented, including the significance of this research and subsequent future work is discussed.

2 MATERIAL PHYSICS OF THE GaN HEMT

In the last chapter WBG power semiconductor materials were introduced. GaN based power devices manipulate the naturally forming Two-Dimensional Electron Gas (2DEG) present across the AlGaN/GaN interface. This chapter will discuss the fundamental development of the AlGaN/GaN heterojunction and its progression towards commercial GaN-on-Si HEMT devices. The structure of the AlGaN/GaN material is explained in detail with particular emphasis on the crystalline unit and piezoelectric and spontaneous polarization charges. In addition, the operation and structural properties of the lateral GaN HEMT power device is examined. Finally, this chapter presents several critical mechanisms of device degradation and their growth techniques.

2.1 The Basic Lateral GaN HEMT Power Device

The basic Gallium Nitride HEMT structure is depicted in figure 2.1. The GaN HEMT device is primarily composed of an AlGaN and GaN layer with suitable terminal contacts. Across the AlGaN/GaN layers exists a heterojunction interface [66]. This "heterojunction" is formed between the two material's dissimilar bandgaps. In this case it is the AlGaN and GaN layers. The property of this heterojunction is key in the operation and identify of GaN HEMT devices. However, like most materials with dissimilar bandgaps large lattice constant mismatches are present. These lattice mismatches can cause high levels of dislocations in the crystal lattice between the two materials. Dislocations (see figure 2.2) heavily effect the operation and reliability of GaN HEMTs and are one of the most prevalent and complex problems surrounding GaN's full market integration. This is why materials with minimal lattice constant differences and large bandgaps differences are desired.
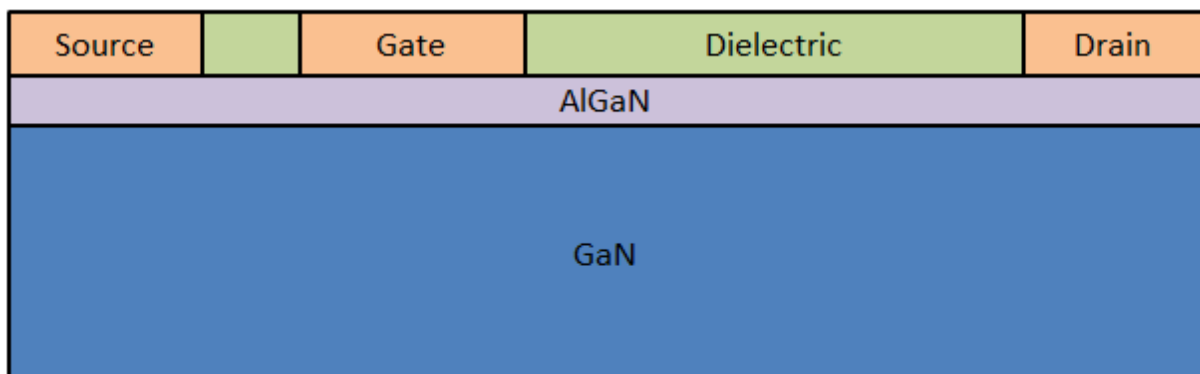
Fig 2-1 The basic GaN HEMT adapted from [67]
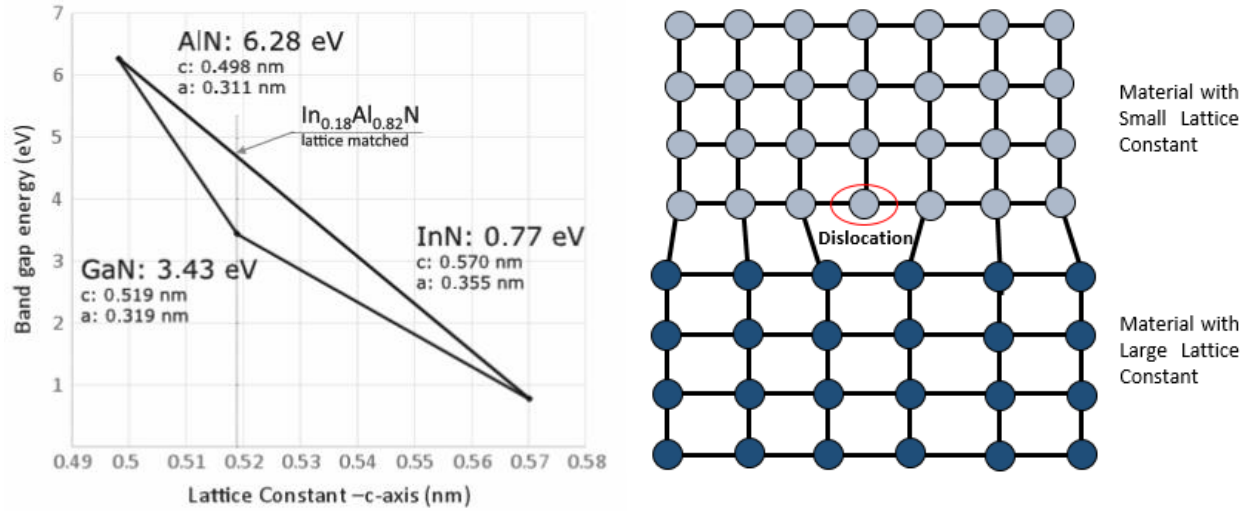
Fig 2-2 Lattice constant vs Band gap energy of group III-Nitrides (left) [16] *and the formation of dislocations (right)*

Figure 2.2 depicts the lattice constant vs bandgap energy properties of AlN, GaN and InN materials. Notice that $In_{0.18}Al_{0.82}N$ has the same lattice constant of GaN and a bandgap difference of approximately 1.27 eV. Dislocations in the $In_{0.18}Al_{0.82}N$/GaN heterojunction would be extremely low and offers a power device that is both capable and reliable. For the conventional AlGaN/GaN HEMT device the Aluminium mole concentration in the AlGaN layer can be altered from pure AlN to pure GaN. However, these extremes offer few incentives so usually the molar concentration of the Al in the AlGaN layer is around 0.25 (25%), with the thickness of this AlGaN layer usually being between 20 - 30 nm thick [68]. This idea of altering the Aluminium mole concentration may be best represented as the following equation;

$$B_{AlGaN}(x) = B_{AlN} * x + B_{GaN} * (1 - x)$$

(Eq.2.1)

Where, *B* denotes the band gap property of the material and *x* refers to the mole concentration. It is therefore, evident that the Al mole concentration has a major influence on the properties of the AlGaN material.

The AlGaN/GaN heterostructure forms what is known as a type I or straddling heterojunction [69]. This is where the bandgap of one material is located within the bandgap of another material, see figure 2.3.
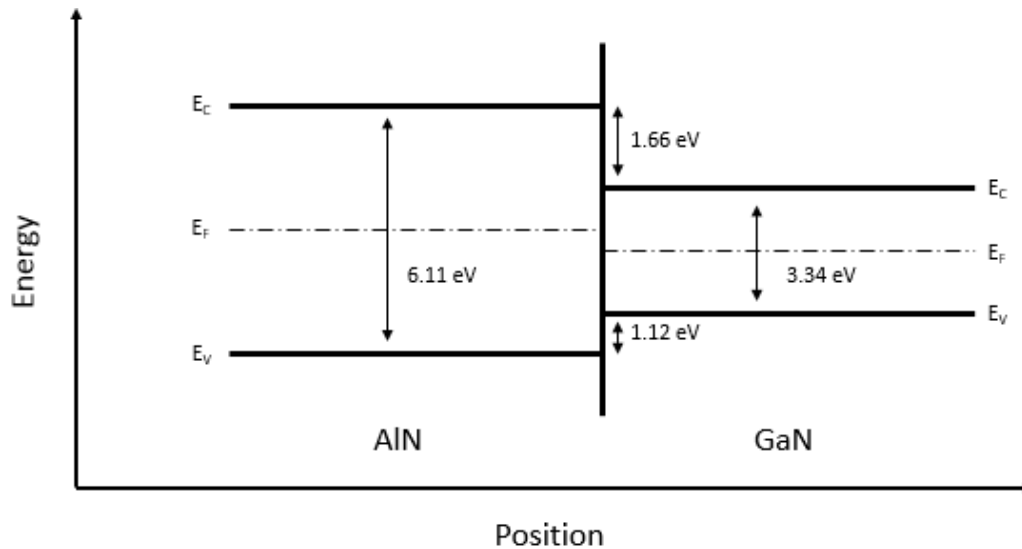
Fig 2-3 Straddling heterojunction band diagram with materials not in contact data used from Tab.A in the appendix

2.2 The Material Physics of AlGaN/GaN

As illustrated in figure 2.1 the basic GaN HEMT power device is comprised of the AlGaN/GaN heterojunction. Before we can address the operation and physical characteristics of a GaN HEMT as a whole, the material physics of AlGaN and GaN must be discussed. The first step is to discuss the properties of the individual components of the GaN material. Gallium Nitride is a compound of Gallium atoms and Nitrogen atoms and is commonly referred to as a group III/Nitride semiconductor. Gallium is a metallic element that has the atomic number 31 and an electronegativity of 1.81 [70]. Nitrogen is a chemical element with the atomic number 7 and an electronegativity of 3.04 [71]. For clarity, the atomic number denotes the number of protons in the atomic nucleus and the electronegativity denotes the attractive force of the atom on chemically bonded electrons and determines the centre of charge in the bond. The Bohr's atomic models for Gallium and Nitrogen are illustrated in figure 2.4.
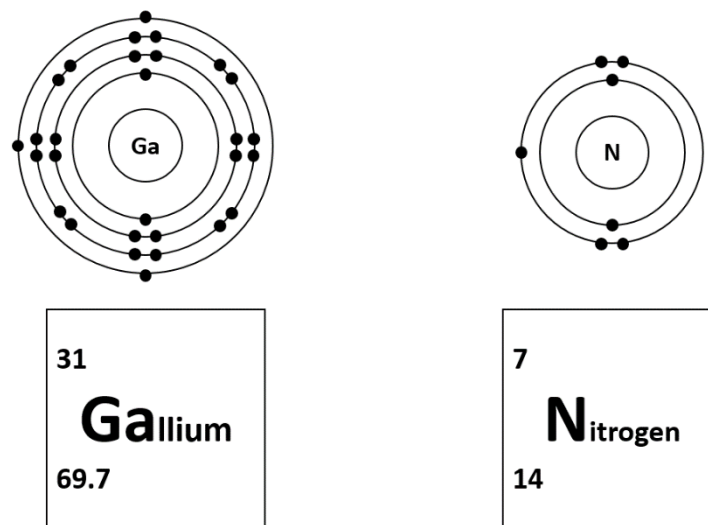
Fig 2-4 Bohr's atomic model for Gallium and Nitrogen with orbital electron positions

Electrons are arranged in shells around the nucleus of the atom. These shells are finite spaces than can be treated as energy levels that electrons can inhabit. The electron configuration for Nitrogen is $1s^2\ 2s^2\ 2p^3$ [71]. For Gallium atoms the electron configuration is $1s^2\ 2s^2\ 2p^6\ 3s^2\ 3p^6\ 3d^{10}\ 4s^2\ 4p^1$ [70]. Atoms naturally tend to the most energetically stable condition. Atoms therefore, want to maintain a full outer shell and easily form compounds that allow this. Looking at the Wurtzite structure (which will be discussed in 2.2.1) Gallium and Nitrogen form four chemical bonds. Three of these bonds are ionic in nature due to the electronegative differences between these elements. The fourth bond is a dative covalent bond, which is a bond formed through Nitrogen donating the 2 electrons inhabiting the first s orbital. The presence of the partial ionic bonds in Gallium Nitride produces Ga cations and N anions. Subsequently, polarisation is present within the unit cell.
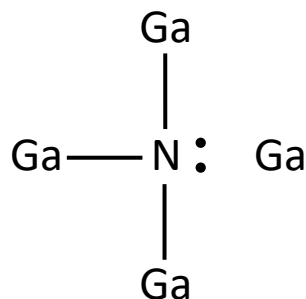
Fig 2-5 The ionic and covalent bonds of GaN

2.2.1 Crystal Lattice Arrangement of AlGaN/GaN

As previously discussed, GaN is a compound of Gallium and Nitrogen. Like most compounds GaN can exist in several forms. The structure of GaN, like all group III-Nitride semiconductors, commonly exists in three different crystalline structures; Rock salt, Zinc Blende and Wurtzite [72], as shown in figure 2.6. Under normal atmospheric conditions the Wurtzite crystal structure is the most thermodynamically stable for group III-Nitrides, therefore, the Wurtzite GaN structure has been adopted as the basis for power electronic switches. Thin GaN films have also been grown in the Zinc Blende crystalline structure [73]. However, Rock salt on the other hand has yet to yield any electronic importance so far as it requires extreme pressures in the range of 40-60 GPa [74] to become thermodynamically stable and cannot be produced by epitaxial growth.
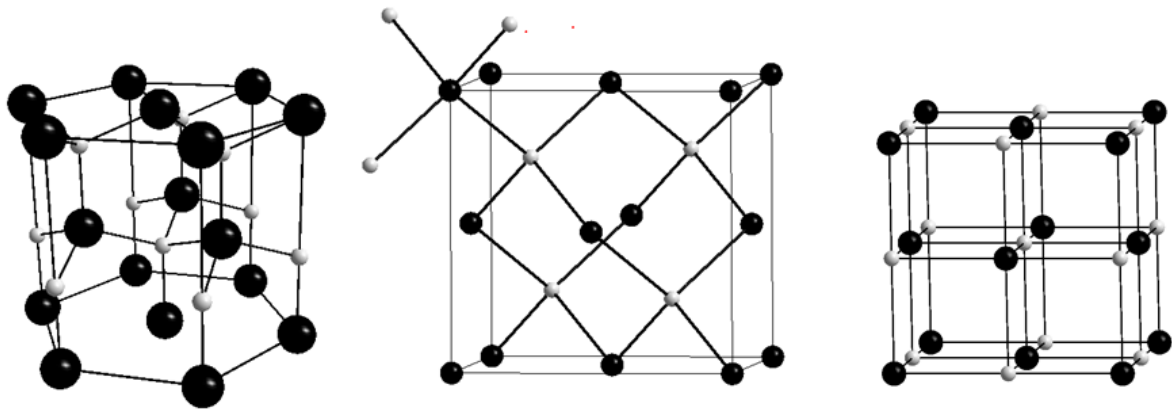
Fig 2-6 Common crystalline forms of group III-Nitrides Wurtzite (left), Zinc Blende (Centre), Rock Salt (right)

The atoms in the crystalline structure of Zinc Blende can be seen as situated in the centre of a tetrahedron with the four nearest atoms forming the corners; this structure creates two interlacing cubic sub-lattices which are offset by 25% along the body diagonal distance [75]. It should be noted that for the purpose of this thesis, GaN in the Zinc Blende form will not be discussed further, instead the Wurtzite crystal structure will be the main focus. Wurtzite is constructed from a crystal unit which has four atoms arranged in what is called a hexagonal Bravais lattice [75]. The parameters of the lattice are defined as the length of a side of the hexagonal base; a, the height; c and the GaN bond length along the c-axis see figure 2.7.
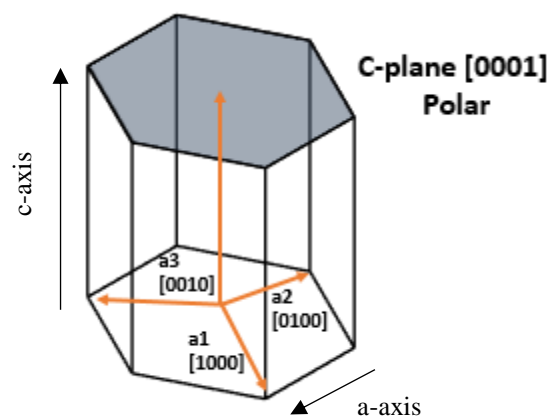
Fig 2-7 The asymmetrical GaN Wurtzite displaying the c-plane, c axis and a axis [76]

2.2.2 Ga and N Face Crystalline Structures

Due to the c-axis, GaN crystals can have Ga or N faces at the cut face. These different faces display different electrical characteristics. Although it should be stated now that Ga face crystals are primarily used.
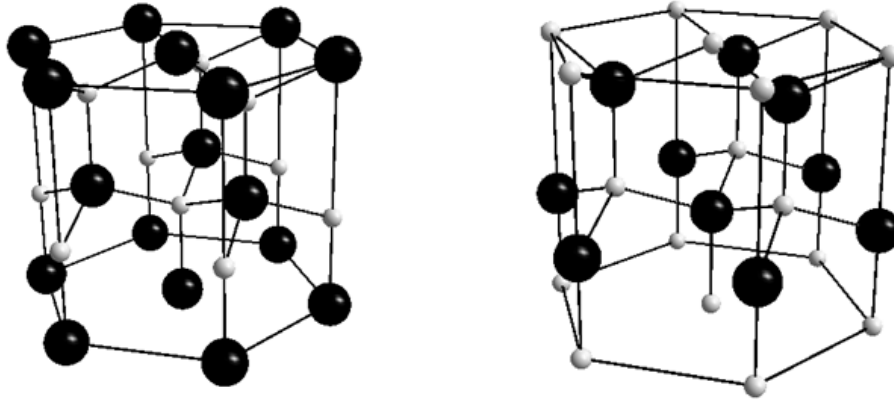
Fig 2-8 Ga face (left) and N face (right) crystalline structures [16]

2.3 The Formation of the 2DEG Channel

GAN crystals, because they have a non-centrosymmetric structure, show different layer sequencing of atoms as they alternate from one side of the crystal to the other. This crystallographic polarity is shown along the c-axis, at 90 degrees to the base plane of the crystal structure and the Ga and N atoms are structured in atomic bilayers. Each of these bilayers is made up of Ga (cation) and N (anion) formed into two closely grouped hexagonal layers. These create polar faces as the difference in electronegativity between atoms which are bonding with each other means that the positive and negative charge centres shifts. Therefore, dipoles with dipole moments are created and the direction will depend on the type of the atoms that are bonding. As GaN devices do not demonstrate symmetry in the c-axis, an inherent electric field is formed due to asymmetry and the formation of a permanent dipole moment will mean that the material is polarised. This Spontaneous polarization does not need any external input, such as an electric field or mechanical deformation [77].

GaN	AlN	InN
0.032 C/m^2	0.029 C/m^2	0.081 C/m^2

Tab 3 The spontaneous polarisation charges in Groups III-Nitrides [78]

Group III-Nitrides including GaN are piezoelectric in nature and therefore, mechanical deformation induces electrical charge. The amalgamation of the AlGaN and GaN layers produce a polarisation charge which is commonly referred to as the piezoelectric polarisation. The mechanical strain is caused when semiconductor crystalline lattices overlay but have different lattice constants and this creates piezoelectric polarization at the interface, GaN devices can experience piezoelectric polarization much higher than Gallium Arsenide (GaAs) and an electron density almost four to five times higher than GaAs [79]. As the proportionality between external stresses and internal deformation is determined by the elasticity of a material, the elastic properties of these materials must be studied so that the operation and reliability of devices grown on such layers can be ascertained. As shown in figure 2.9 the resultant internal polarisation vectors equal zero when no external mechanical force is applied. When external mechanical force is applied to crystal unit the resultant charge is equal to the piezoelectric polarisation.
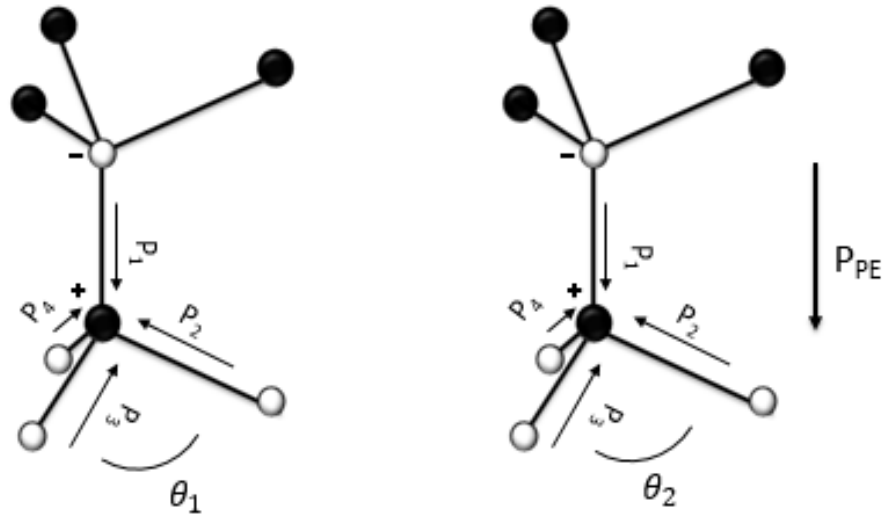
Fig 2-9 The
piezoelectric polarisation effect in GaN no stress (left) and in AlGaN with tensile stress (right)

Equation 2.2 represents the effective piezoelectric polarisation with no external stress.

$$P_1 + P_2 + P_3 + P_4 = 0$$

(Eq.2.2)

Equation 2.3 represents the effective piezoelectric polarisation with external stress when $\theta_{1\neq}\theta_2$;

$$P_1 + P_2 + P_3 + P_4 = P_{PE}$$

(Eq.2.3)

The piezoelectric charge density can be theoretically calculated as shown in figure 2.10.
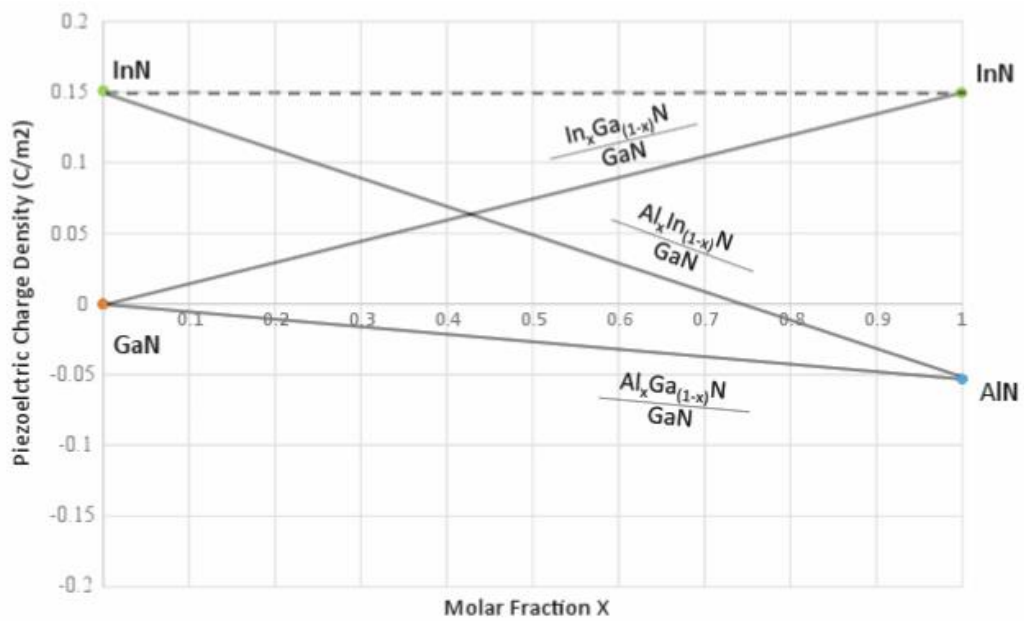
Fig 2-10 Theoretical effective piezoelectric charge density for AlGaN, InGaN and AlInN over GaN [80]
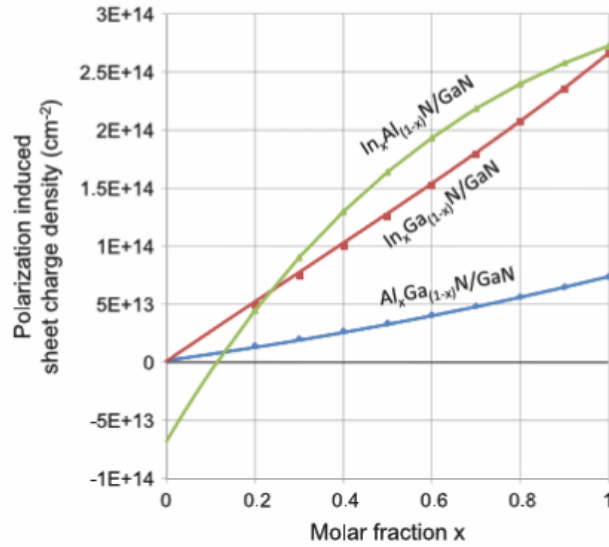
Fig 2-11 Theoretical effective carrier density of at the heterojunction interface of the spontaneous and piezoelectric polarisation charge density for AlGaN, InGaN and AlInN over GaN [81]

The resultant mechanical stress can therefore, induce a large positive charge across the heterointerface. The subsequent positive charge generates electrons to maintain charge neutrality. This phenomenon produces a highly concentrated 2-Dimensional Electron Gas (2DEG) across the junction in a quantum well.

For the undoped AlGaN/GaN heterojunction the formation of the 2DEG can be explained with the introduction of donor states on the AlGaN surface. Fig 2.12 illustrates the energy band gap of an isolated AlGaN material with the introduction of surface donor states. It is assumed that the isolated AlGaN material is under no tensile/compressive strains. Providing that the AlGaN material is thick enough, (i.e. meaning more positive polarisation charges) the Fermi level Once the fermi level reaches the donor state level Es, the electrons are promoted to the conduction band and are drawn to the other side by the polarisation induced electric fields. As the AlGaN and GaN materials come into contact with each other, the fermi level causes the electrons to drop into the GaN side. This accumulation of electrons at the interface forms what is known as the 2DEG (shown in fig 2.13.) and this, together with the ionized surface donor generates an electric field which points from the interface to the surface and reduces the polarisation field in the AlGaN layer [82].
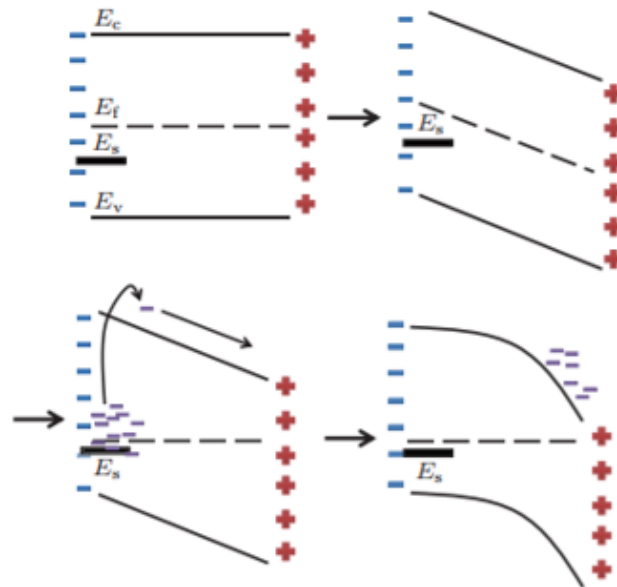
Fig 2-12 The energy band of a undoped AlGaN material with E_s surface donor states. Electrons are promoted into the conduction band and tend to the positive polarisation induced electric field [82]
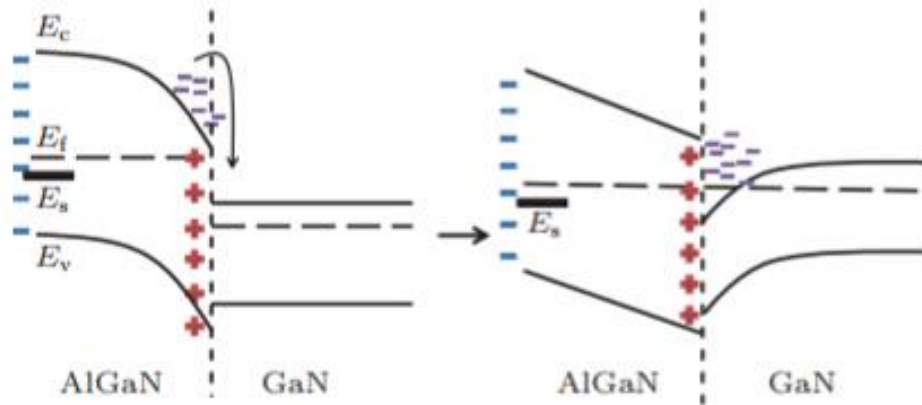
Fig 2-13 The energy band of an undoped AlGaN/GaN heterojunction displays the accumulation of the electrons in the 2DEG quantum well [82]
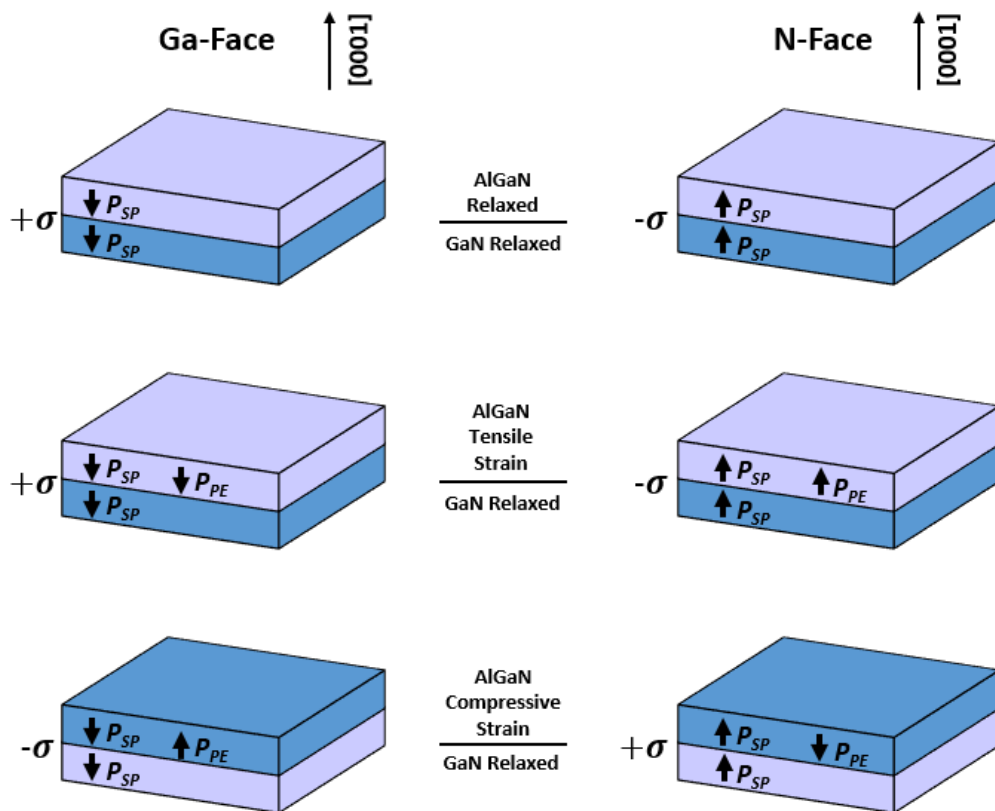
Fig 2-14 Polarisation induced sheet charge densities and directions of the spontaneous and piezoelectric polarisations in Ga-face and N-face strained and relaxed AlGaN/GaN heterojunction redrawn from [81]

The Heterojunctions formed by GaN materials can be characterised by the bound charge. The bound charge is the summation of the spontaneous polarisation and the piezoelectric polarisation. The formation of GaN HEMT allows different combinations of strained layers. If the bound charge is positive at the AlGaN/GaN heterojunction, free electrons are attracted to this this heterojunction and form the 2DEG channel. For the purpose of this thesis the Ga face, AlGaN under strain /GaN heterojunction is used.

2.4 The Development of the Basic Lateral GaN HEMT Power Device

As discussed in the previous section the spontaneous and piezoelectric polarisation charges present in the AlGaN/GaN heterojunction forms a quantum well that electrons are attracted to and create a highly dense 2DEG channel. This 2DEG channel is critical for in the development and operation of lateral GaN HEMTs. The electron density in this channel can be mathematically calculated through simultaneously solving the Schrödinger and Poisson equations. The inherent sheet electron density of the 2DEG can be calculated by;

$$N_s = \frac{\sigma(x)}{e} - \langle \frac{\epsilon_0 \epsilon(x)}{d_{AlGaN} e^2} \rangle \ [e\phi_b(x) + E_{CF}(x) - \Delta E_C(x)]$$

[83]

(Eq.2.4)

Where, d_{AlGaN} is the thickness of the AlGaN barrier layer, $e\phi_b$ is the Schottky barrier height in eV, E_{CF} is the penetration of the conduction band edge below the Fermi level at the AlGaN/Interface and E_C is the conduction band offset at the AlGaN/GaN interface.

$\Delta E_C(x)$ can be calculated through

$$\Delta E_C(x) = 0.7[E_g(x) - E_g(0)]$$

(Eq.2.5)

$E_{CF}(x)$ can be calculated through

$$E_{CF}(x) = E_0(x) + \frac{\pi \hbar^2}{m^*(x)} n_{2DEG}(x)$$

(Eq.2.6)

2.4.1 The Band Diagram for the Basic Lateral GaN HEMT

Understanding and taking the material parameters, band diagrams can be formed to represent the effective electrical properties of devices.
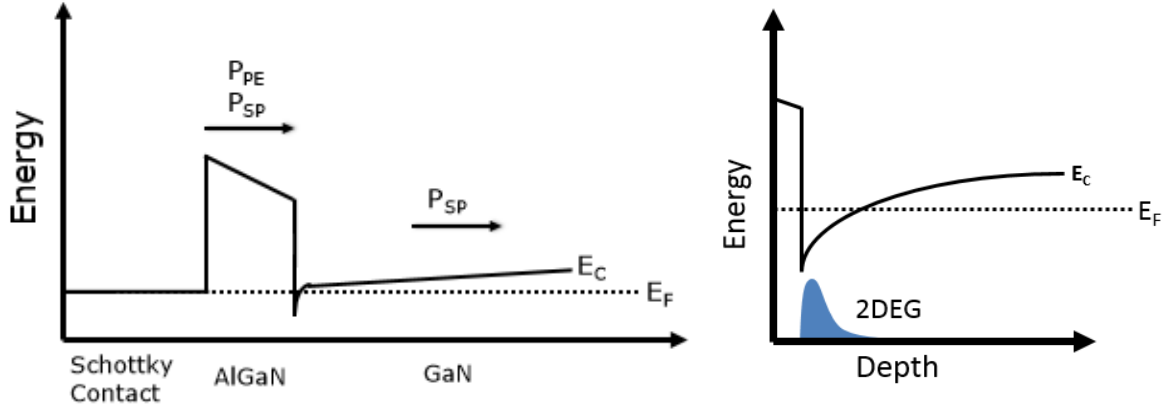
Fig 2-15 The Band diagram of a Schottky-AlGaN/GaN heterojunction (left) and the 2DEG concentration in the quantum well (right)

Analysing the band diagram in figure 2.15 the threshold voltage for the AlGaN/GaN HEMT can be determined.

$$V_{TH} = \phi_b - \Delta E_C - V_{AlGaN} = \phi_b - \Delta E_C - \frac{qN_s d_{AlGaN}}{\epsilon_0 \epsilon_{AlGaN}}$$

[16]

(Eq.2.7)

Where $e\phi_b$ is the Schottky barrier height, E_C is the conduction band offset, N_s is the 2DEG density, d_{AlGaN} is the thickness of the AlGaN barrier layer, ϵ_{AlGaN} is the relative dielectric constant of AlGaN and q is the electron charge.

From this we realise that the AlGaN/GaN HEMT is normally-on due to the negative threshold voltage and therefore, we described them as Depletion mode (D-mode) devices. Normally-on devices are not desirable in power electronics as system designs need to be made more robust to stop accidental turn on events. This is where equation 2.7 is extremely useful again, as this enables engineers to develop solutions for normally off devices known as Enhancement mode (E-mode) devices. The variables that this equation allows to be altered are;
1. Increasing the work function of the Schottky contact.

2. Lowering the Aluminium mole concentration in the AlGaN layer.

3. Reducing the thickness of the AlGaN layer

[16]

These principles have led to the development of several E-mode devices such as the p-type GaN Gate Injected Transistor (GIT). Although, this is not the only way to obtain a device with a E-mode operation, composite devices which manipulate the D-mode GaN HEMT using an E-mode Si MOSFET have also been developed. In addition, Fluorine implanted devices have also been proposed. These concepts will be discussed in greater detail in chapter 3.

2.4.2 Properties and Operational Aspects of the Lateral GaN HEMT
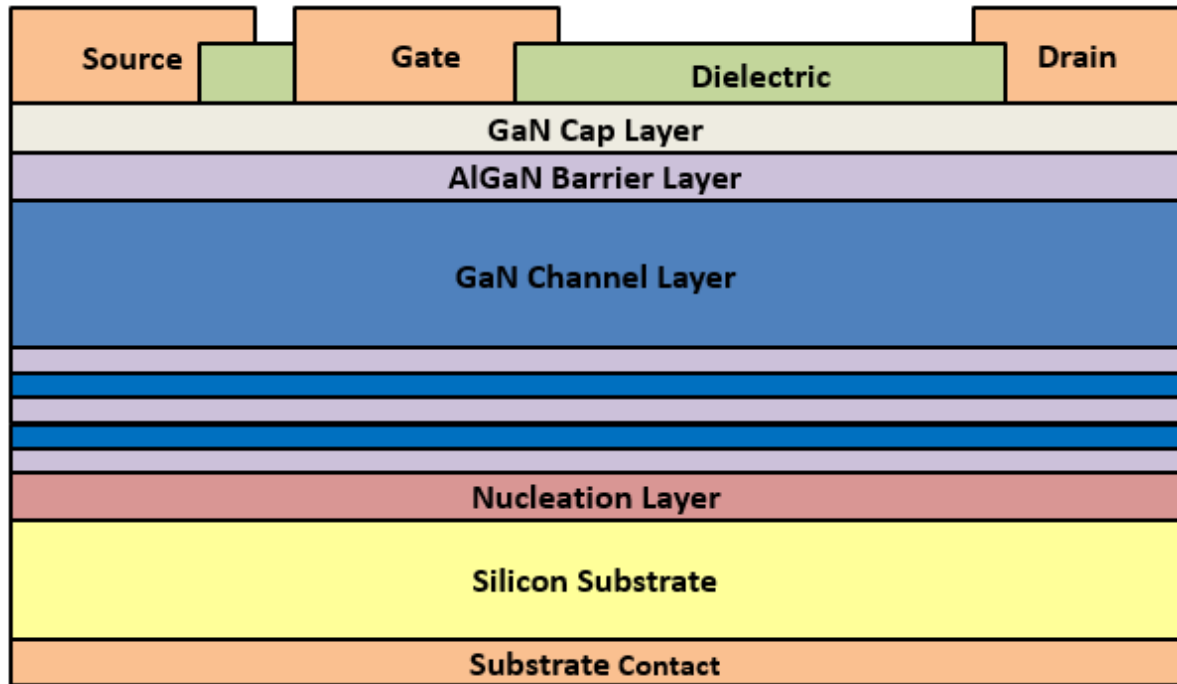
Fig 2-16 A more advanced design of a GaN HEMT power device

As previously identified the properties of GaN HEMT devices are not only dependant on the material properties but the device structure. In literature the electron mobility for bulk GaN is 440 cm^2/Vs [84]. However, the GaN HEMT operates using the 2DEG that is formed in the quantum well between the heterojunction interface. This quantum well provides electrons with a highly conductive channel, allowing high electron mobility. It is reported in literature that the electron mobility in GaN HEMT devices can be upwards of 1500 cm^2/Vs [85]. The use of AlN in the barrier layer allows large carrier density even at reportedly low barrier thicknesses. Literature reports even for 3.5 nm the carrier density in the 2DEG channel is 2.8x10^{13} cm^{-2} [86]. However, surface sensitivity, high leakage currents and high Ohmic contact resistances have restricted this progression. It should be noted that GaN HEMT has been heavily used in Radio Frequency (RF) applications before power electronic applications so much of the development has been completed in this field. Group III-Nitrides with inherent piezoelectric and spontaneous polarization charges do not need additional n-type doping and doping GaN with p-type dopants is not readily achievable and has thus limited the development of vertical GaN power devices. The next sections briefly describe the structural properties of the GaN HEMT shown in figure 2.16.

2.4.2.1 Terminal Contacts

Beginning at the outer components of the GaN HEMT, figure 2.16 depicts four terminals; the source, gate, drain and substrate. The source, drain and substrates terminals are all ohmic in nature. The gate terminal however, is a Schottky Barrier contact and controls the device by manipulating the 2DEG channel underneath. The source gate and drain terminals have field plate technology incorporated into their design. Field plates actively redistribute the electric field lines in the device and divert them away from the terminal edges which are extremely susceptible to degradation. Field plate technology for GaN devices is becoming more mature and as a result the latest generation of devices have significant reductions in field plate sizes.

2.4.2.2 Dielectric Layers

The dielectric layers or sometimes more commonly referred to as the passivation layers are usually Si$_3$N$_4$. This layer has been introduced to the GaN HEMT to enable the construction of field plate technology, as well as to

prevent current collapse. Current collapse or dynamic R_{ON} is attributed to these surface traps and the implementation of this passivation layer discourages this. These surface traps and the subsequent current collapse are discussed in further detail in section 2.5.

2.4.2.3 Cap Layer

GaN HEMT devices commonly have what is known as a cap layer grown on top of the AlGaN barrier layer. The cap layer is typically a layer of GaN with a thickness of a few Nano meters. This layer serves several purposes including the prevention of oxidation, provision of a low resistance path for the terminals, redistribution of the electric field lines and minimising the leakage current across the gate to Schottky terminal. The presence of GaN cap layer also produces a Two-Dimensional Hole Gas (2DHG) channel.

2.4.2.4 Barrier Layer

The barrier and channel layer are effectively the heterojunction structure describe in section 2.1. The barrier layer is an essential component of the GaN HEMT device. This layer is composed of an AlGaN material. The AlGaN barrier layer has a wider band gap than that of the GaN channel layer so a straddling heterojunction can be formed as discussed earlier.

2.4.2.5 Channel Layer

Likewise, the channel layer is also an essential component of the GaN HEMT device. This layer is composed of a GaN material. The GaN channel layer has a smaller band gap than the AlGaN barrier layer so the straddling heterojunction can be formed. The joining of these two layers produces the 2DEG at the interface.

2.4.2.6 Buffer Layer/Nucleation layers

The buffer/nucleation layers are included to minimise the effects of the lattice mismatch between the GaN and hetero-epitaxial substrate. Effective buffer regions will minimise the cracking, dislocations and the injection of electrons from the Silicon substrate. The arrangement of these layers is somewhat complex and manufactures are sensitive about their designs. However, the designs of these layers are typically arranged in thin AlN, AlGaN and GaN super lattices.

2.4.2.7 Substrate

GaN is usually grown on Silicon substrates because of the low cost, well-established fabrication process and the large wafer diameter production. This attraction is also motivated by the potential for standard CMOS integration. As the lattice mismatch between GaN and Silicon is 17% [87], a significant problem is presented for the effective incorporation of the GaN materials. In addition, Silicon has a thermal conductivity of 1.3 W/cm K [16] which enables a relatively high thermal dissipation compared to other cost effective substrates so allows more efficient thermal performances.

2.4.3 The Operation of the Lateral GaN HEMT Power Device

The GaN HEMT uses the heterostructure and bound charge present between the barrier and channel layers to form a 2DEG channel. This channel allows high electron mobility. It is therefore, evident that the operation of this device is dependent on the manipulation of this 2DEG channel.
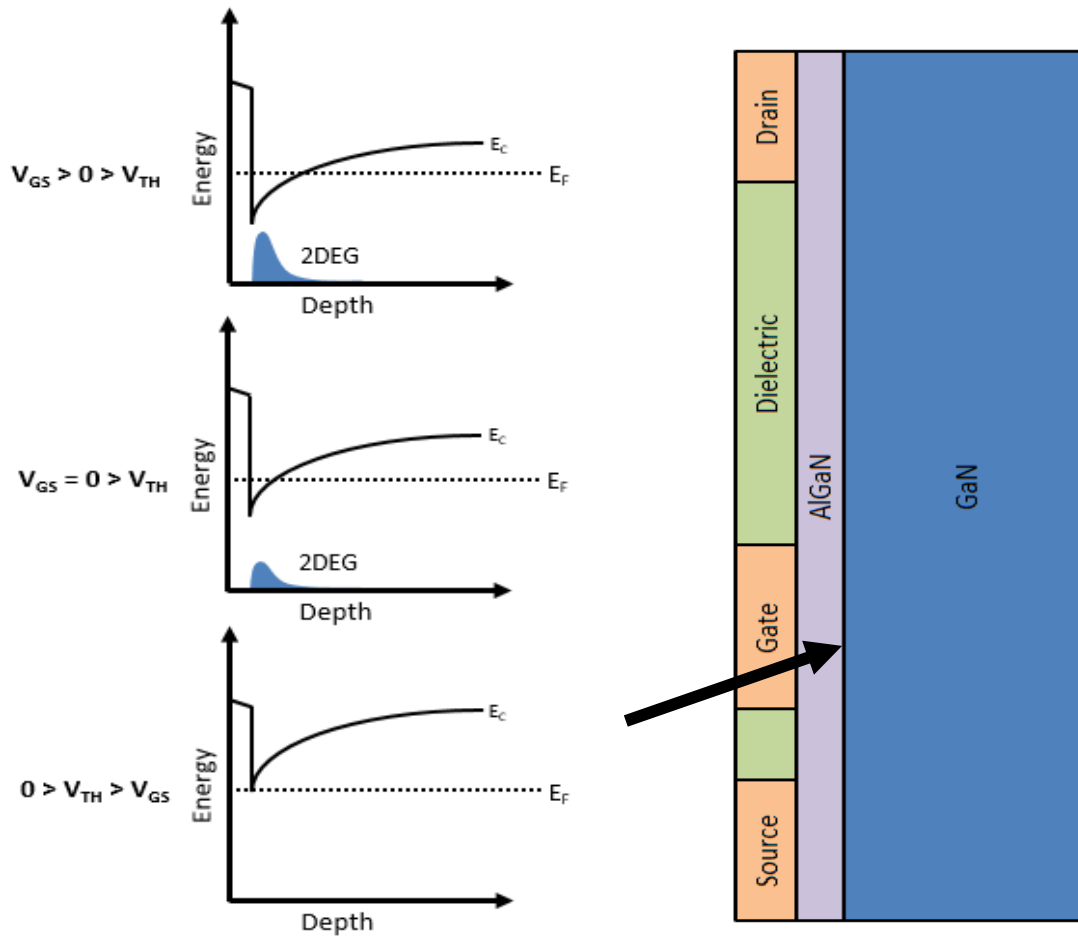
Fig 2-17 The band diagrams for the three locations of the 2DEGs V$_{GS}$ > 0 >V$_{TH}$, V$_{GS}$ = 0 > V$_{TH}$ and 0 > V$_{TH}$ > V$_{GS}$ (left) and the GaN HEMT (right)

2.4.3.1 Zero Bias V$_{GS}$ = 0 >V$_{TH}$

At zero bias the 2DEG channel across the AlGaN/GaN interface is inherently present due to the positive bound charge produced by the spontaneous and piezoelectric charges. However, charge carriers will not flow form the drain to source terminals until a positive voltage bias (V$_{DS}$) is present.

2.4.3.2 V$_{GS}$ > V$_{TH}$

At a gate bias (V$_{GS}$) larger than the device threshold voltage (V$_{TH}$) charge carriers will flow across the 2DEG providing that there is a positive bias (V$_{DS}$) present. However, if the V$_{GS}$ exceeds the Schottky barrier threshold electrons flow between the gate and source terminals. This drastically reduces the drain current.

2.4.3.3 V$_{GS}$ < V$_{TH}$ < 0

When the gate bias is smaller than that of the GaN HEMTs threshold voltage, the channel underneath the gate is pinched off. The incomplete current path means that the electrons do not have a current path and therefore, the drain current is approximately zero. This operational mode is generally referred to as the off-state.

2.5 Degradation of Lateral GaN-on-Si HEMT Power Devices
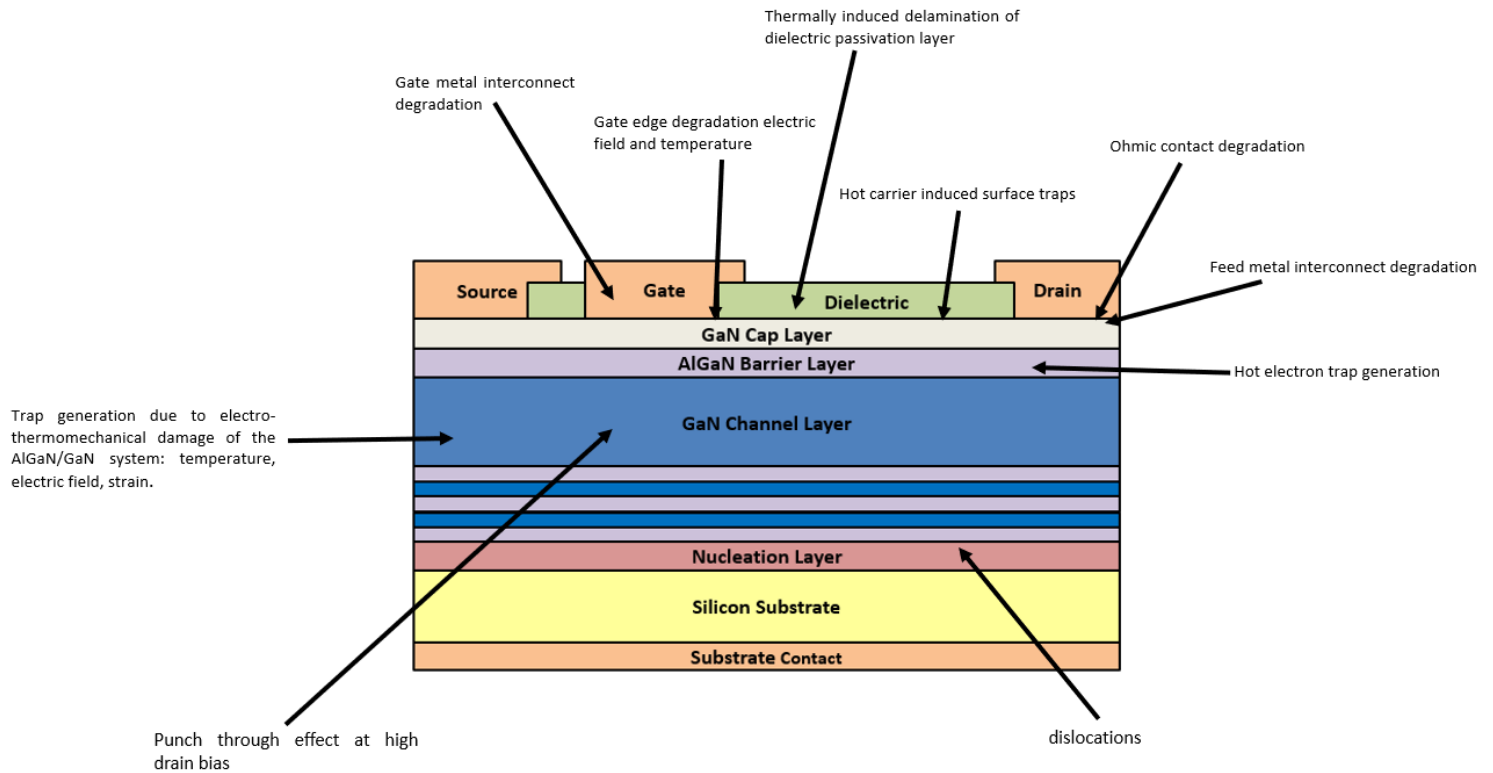
Fig 2-18 A power GaN HEMT with common types of traps/degradation and locations [88]

Degradation in GaN devices is very complicated and covers a broad spectrum of topics that are still in their infancy. However, one of the first successes in terms of device performance came in the form of Si_3N_4 passivation layers.
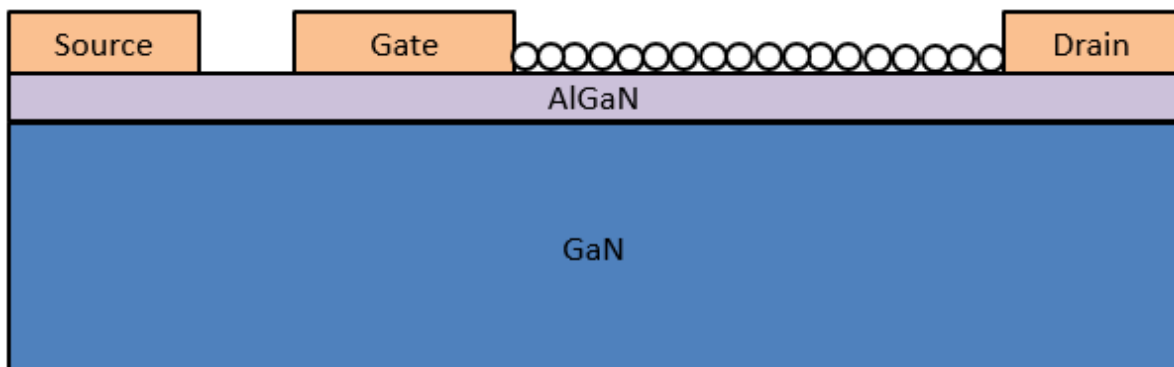
Fig 2-19 A GaN HEMT under zero bias with no passivation layer and unfilled surface traps.

The white circles on the AlGaN surface layer in figure 2.19 and 2.20 represent unfilled surface traps. When a negative gate voltage occurs i.e. turning the device off electrons are leaked by the gate and are held by the surface traps. These surface traps which are now full are represented by the black circles in figure 2.20. The electrons trapped in these surface traps will behave as a "virtual gate" [89]. This virtual gate depletes the 2DEG underneath them by pinching it off. Electrons can be held in these traps for relatively long periods due to the time in which to detrap and if the gate bias returns to zero the 2DEG may still be slightly depleted due to the trapped electrons acting as a virtual gate. This concept is what is commonly referred to as current collapse as this dramatically reduces the drain current, effectively increasing the R_{ON}.
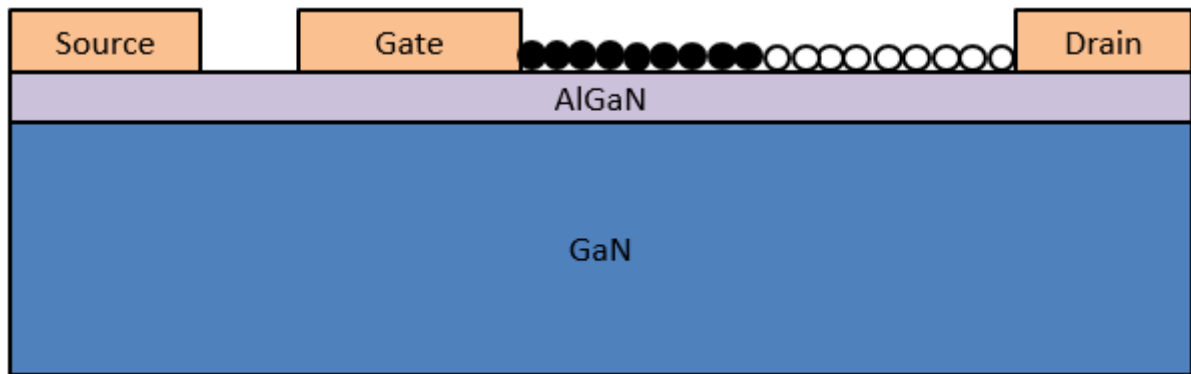
Fig 2-20 A GaN HEMT under negative gate bias with no passivation layer and partially filled surface traps forming a "virtual gate"

This phenomenon has led to the development of Si_3N_4 passivation layers. The Si_3N_4 acts as shallow donors in these surface traps. This prevents the virtual gate from forming and minimises current collapse attributed to the surface states.
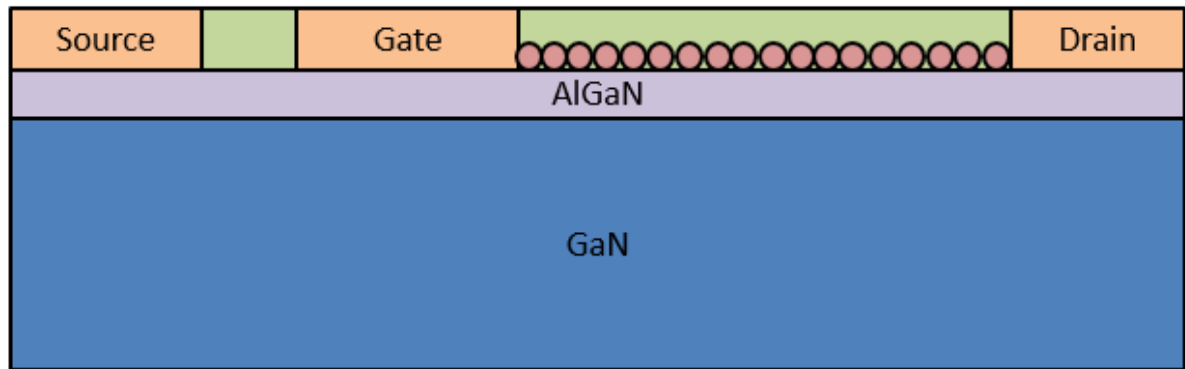
Fig 2-21 A GaN HEMT with a passivation layer and Si₃N₄ passivation

Current collapse or dynamic R_{ON} can be represented through the I-V characteristics illustrated in figure 2.22 and is temporary state with the device's R_{ON} returning to its initial state.
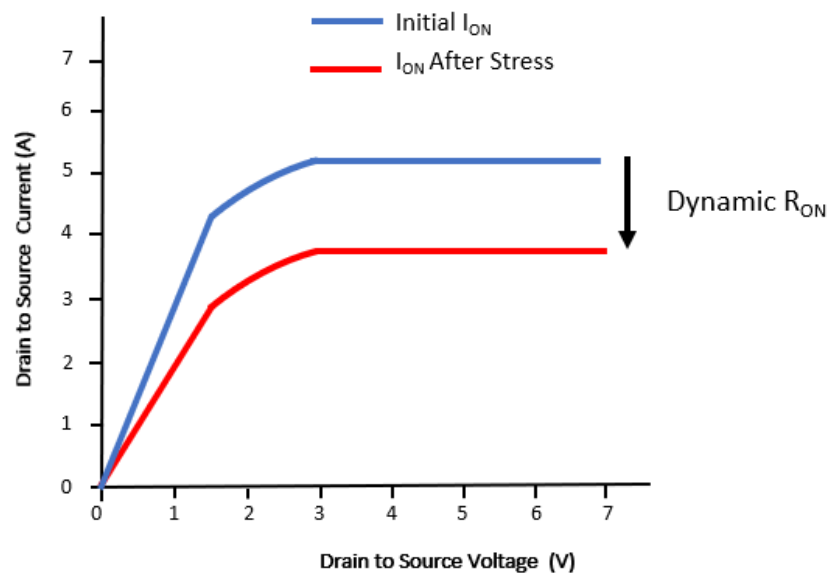
Fig 2-22 GaN dynamic RON after High Temperature Reverse Bias Stress

2.5.1 Reliability Standards for GaN Based Power Devices

It has been extensively reported that the electric field strength at the edges of the gate and drain contacts cause degradation in GaN HEMTs [89]. Field plates have therefore, been widely adopted to redistribute the electric field strength away from these locations. There is no universal reliability standard in the field of power devices. However, JEDEC standards are widely used by manufactures to ensure reliability levels. It is no wonder that more conventional power devices including the MOSFET are usually tested in conjunction to JEDEC standards. JEDEC standards encompass a wide range of device and packaging related tests including; High Temperature Reverse Bias (HTRB), High Temperature Gate Bias (HTGB), High temperature storage, temperature cycling, high temperature high humidity reverse bias, unbiased autoclave, moisture sensitivity level and electrostatic discharge experiments. However, the nature of these experiments were developed for traditional Silicon power devices and as GaN HEMT devices like most WBG power semiconductor display different prominent breakdown mechanisms the validity of these experiments has been called into questioning [90] and JEDEC have even began the JC-70 committee to develop new experimental testing standards for WBG devices [65]. Another challenge with WBG materials is accelerated life time tests. Well established models are used for traditional Silicon power devices. These models have not been confirmed for GaN devices as these devices have only recently been commercialised. It should also be stated that the qualifications procedure for lateral and vertical GaN power devices will probably be different.

2.6 Growth Techniques for GaN HEMT Based Power Devices

The epitaxial growth of GaN can be performed in several different techniques however; by far the most common is MBE molecular beam epitaxy, MOCVD and HVPE. MOCVD is in fact the most universal technique for the growth and fabrication of GaN epilayers. For MOCVD growth of GaN temperatures upwards of 1000℃ are typically used [91]. The technique of MOCVD encompasses the use of reactants in gas form, such as Trimethyl-Gallium and Ammonia [92]. The gases are passed over heated substrates (usually Silicon) and react to form condensed layers micro meters thick on the substrate. MOCVD techniques have a growth rate of about 2 micro meters an hour [92].

MBE techniques allow the use of solid GaN and AlN materials in conjunction with ammonia. The reaction of these materials occurs in a high vacuum reactor. MBE is used for the growth of single crystals and allows precise growth at the heterojunction. The advantages of this technique are the growth of monolayers with precise thickness and doping concentrations. In traditional MBE techniques Al and GaN are reacted using a effusion cells at high temperatures. This allows the reactants to grow in thin films. The process is automated so precise control of thickness of the layers is obtained. The growth rate for MBE is typically around 1 micro metre and hour [91]

For GaN HEMT devices the epilayers are typically hetero-epitaxially grown. The most common and viable solutions for this are Sapphire, SiC and Si substrates. The reason why GaN is not homo-epitaxially grown is the economical and complex nature in developing large amounts of GaN substrates, although [93] reported progress in the growth of bulk GaN. That being said if GaN substrates are eventually made viable, the performance and reliability of these devices will rapidly increase. As the probability of dislocations will be dramatically reduced and breakdown mechanisms that are currently seen in GaN products due to the Si substrate will not be present. As mentioned before Si is the most attractive substrate and one that power electronic engineers have pushed for commercial applications.
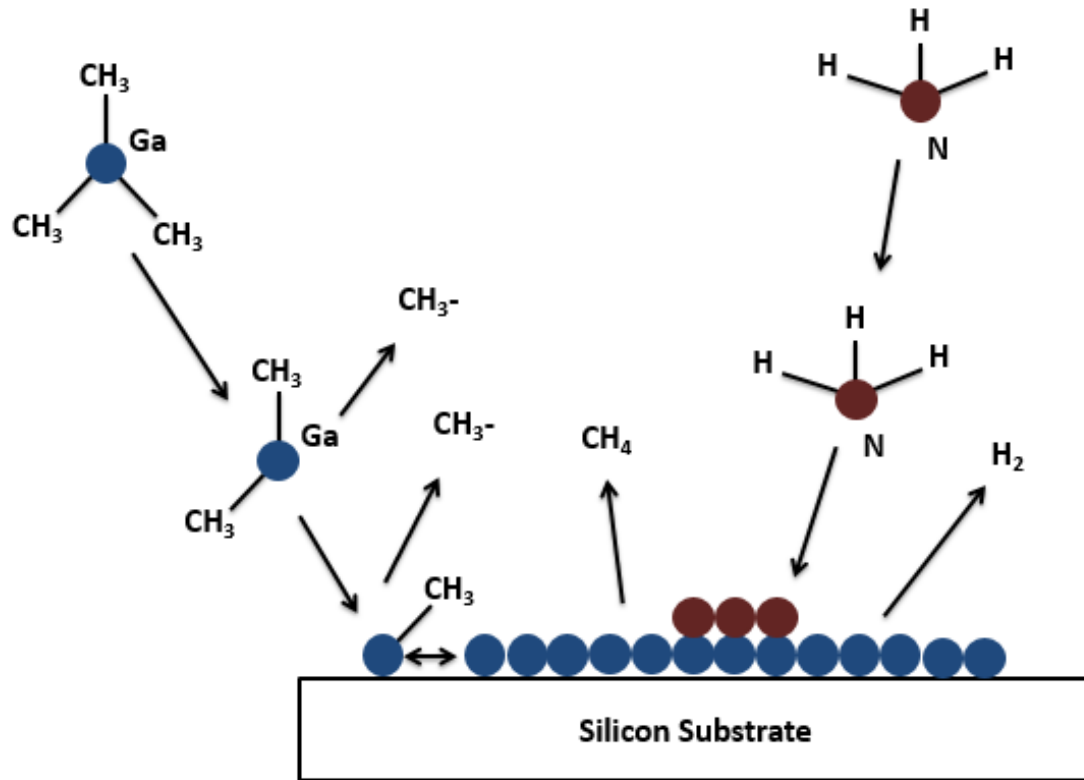
Fig 2-23 GaN being epitaxially grown using MOVCD on a Silicon substrate

In figure 2.23 the following chemical equations take place;

$$(CH_3)Ga(g) + NH_3 \rightarrow GaN(s) + 3CH_4(g)$$
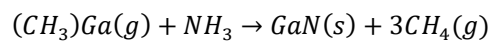
(Eq.2.8)

However, for the growth of fractional compounds like AlGaN, Trimethyl-Aluminium is reacted with Trimethyl-Gallium and Ammonia at elevated temperatures as shown in Equation

$$x(CH_3)_3Al + (1-x)(CH_3)_3Ga + NH_3 \rightarrow Al_xGa_{1-x}N + \cdots$$
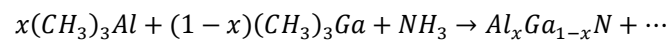
(Eq.2.9)

Where; x is the mole concentration, $(CH_3)_3Al$ is Trimethyl-Aluminium, $(1-x)(CH_3)_3Ga$ is Trimethyl-Gallium, NH_3 is Ammonia and $Al_xGa_{1-x}N$ Aluminium Gallium Nitride with mole concentration.

2.7 Development to Commercial GaN-on-Si Power Devices

GaN-on-Si based power devices have displayed remarkable progression within recent years [94]–[97]. As previously discussed GaN HEMTs are inherently D-mode devices meaning under zero gate voltages they are normally-on. GaN-on-Si D-mode devices have imposed significant challenges to system engineers to provide safety measures that inhibit complications like shoot-through failures arising [98]. This has motivated manufactures to develop several Enhancement mode devices as reported by [99]. For this thesis the Transphorm cascode GaN-on-Si and Panasonic GaN-on-Si GIT is considered as arguably these are the most promising GaN technologies currently available [100].

After development Panasonic commercialised the 600 V PGA26C09DV p-GaN GaN-on-Si GIT in 2013 [101]. At the same time Transphorm presented the first qualified data for a cascode GaN-on-Si HEMT device in 2013 [102]. Not long after that Transphorm began to produce the first generation of commercially available GaN-on-Si cascode HEMTs. An extensive table of GaN-on-Si power devices can be found in the appendix A.

2.7.1 The Panasonic GaN-on-Si Gate Injected Transistor

The distinction between these devices lies in how they obtain Enhancement mode operation. The Panasonic GIT is an inherently normally-on device the schematic for this device is shown in figure 2.24. The GaN GIT utilises a p-doped GaN layer underneath the gate terminal to shift the potential at the heterojunction interface in line with the gate [55] as shown in figure 2.25. The Panasonic GIT also has an p-GaN region adjacent to the drain that is used to prevent the phenomenon of dynamic R_{ON} by detrapping electrons [103]. The structure of the GaN GIT resembles that of the structure of a Junction Field Effect Transistor JFET however; the GaN GIT experiences conductivity modulations at high gate voltages.
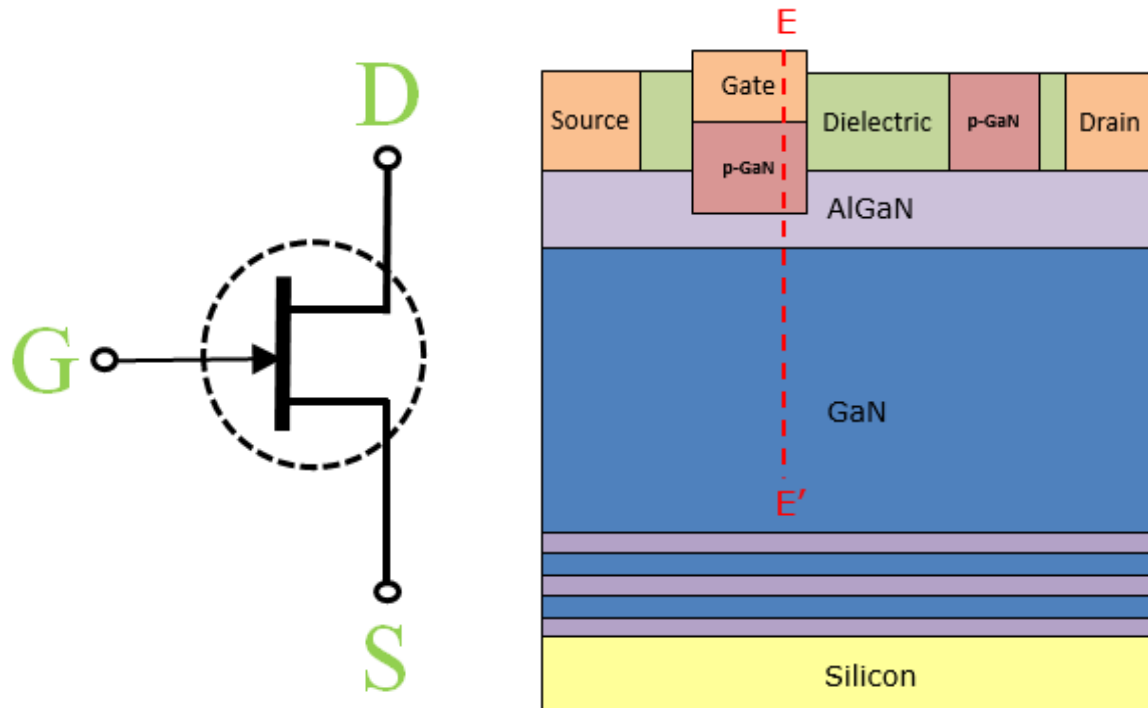
Fig 2-24 A GaN GIT's circuit schematic (left) and structural diagram (right)

In figure 2.25 the quantum well underneath the gate has been lifted above the fermi level and hence is not normally-off.
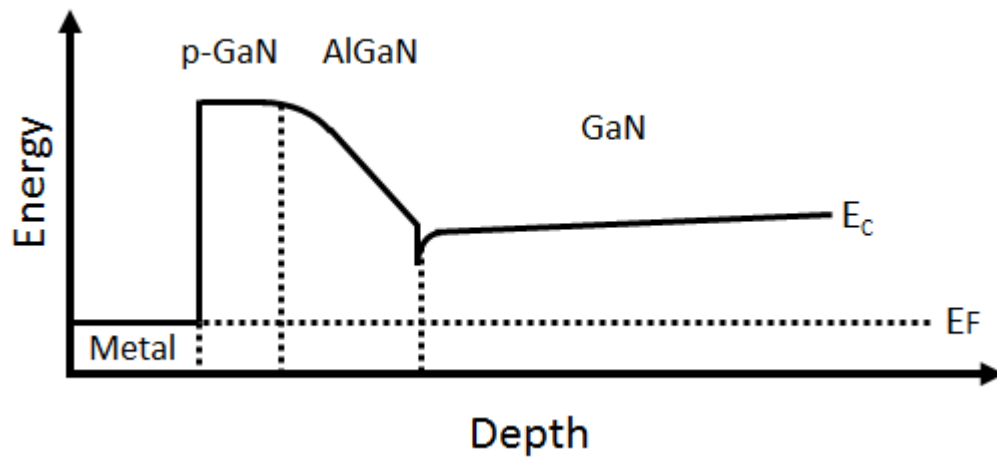
Fig 2-25 The band diagram for the Panasonic GaN-on-Si GIT [55]

Figure 2.26 displays the GaN-on-Si GIT die for a Panasonic PGA26E19BA due to being an inherently E-mode device this device is far smaller than the cascode device presented in section 2.7.2.
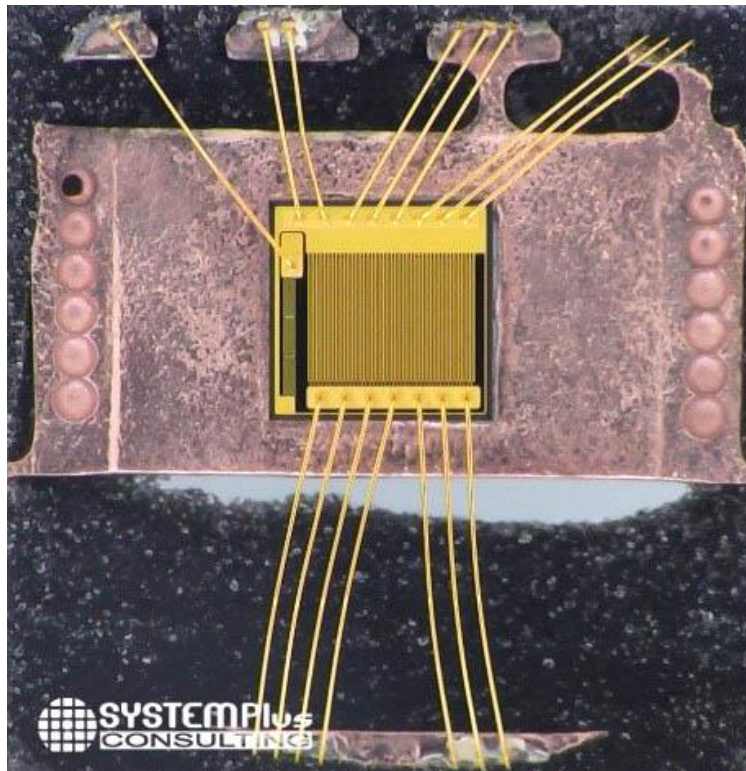
Fig 2-26 Panasonic PGA26E19BA GaN-on-Si GIT [104]

2.7.1.1 Operation of the GaN-on-Si GIT

At zero gate bias the 2DEG underneath the p-doped region is fully depleted and therefore, the channel does not allow the movement of carriers. When the gate bias is increased the drain current slowly begins to increase. Once the gate bias passes the built in potential of the p-n junction holes are injected into the 2DEG from the p-doped region. This phenomenon is called the conductivity modulation this also means a subsequent increase in carriers in the channel due to charge neutrality. This allows very low on resistances for this device. The injected holes can be assumed to be static as their mobility is negligible compared to the electron mobility. The conductivity modulation in GaN-on-Si GITs maybe best described figure 2.27. (a) The 2DEG is depleted under the p-GaN/gate region at zero bias. (b) The p-GaN layer injects holes into the 2DEG. (c) Holes attract additional electrons form the channel layer into the 2DEG. (d) The GaN GIT 2DEG has additional charge carriers and therefore reduced R_{ON}. It should be stated that because the hole mobility is so low for GaN the holes can be treated as static entities and the p-GaN region beneath the gate is recessed so that the p-GaN adjacent to the drain does not inject holes into the 2DEG.
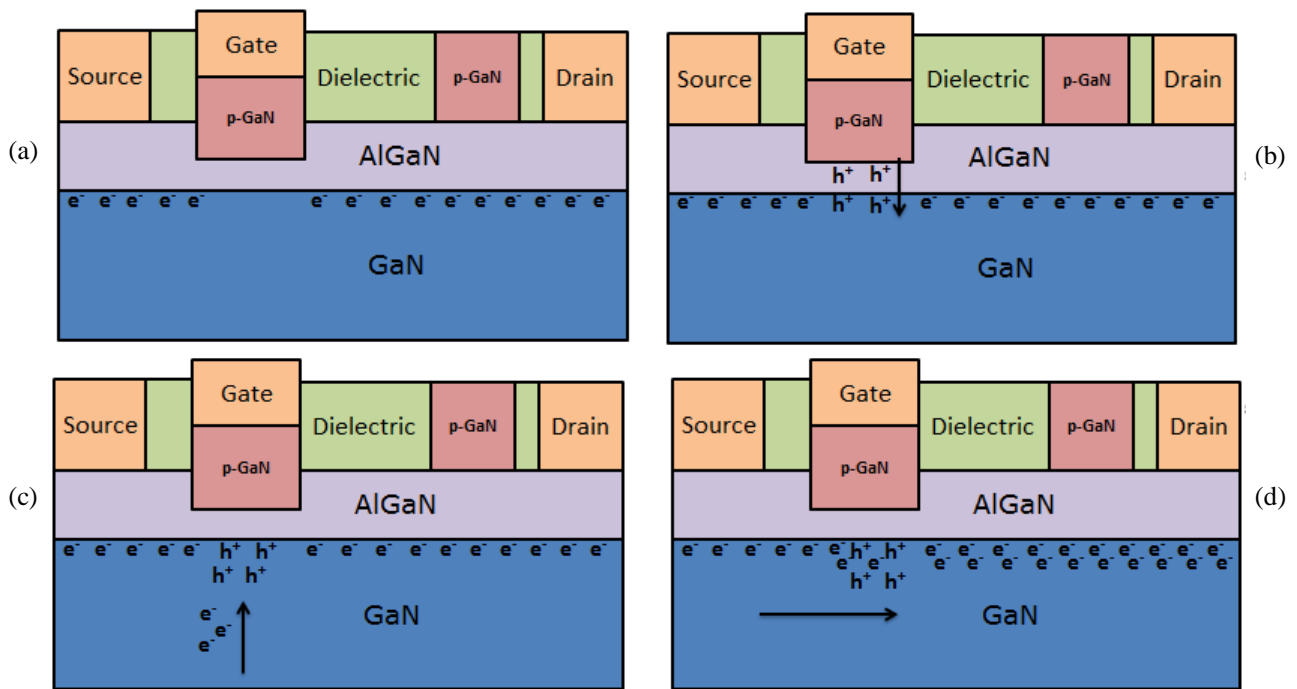
Fig 2-27 The conductivity modulation in GaN-on-Si GIT devices

The p-GaN layer on the right of figure 2.28 is connected to the drain terminal. This therefore, means that when a high reverse bias is applied to the drain terminal holes are injected from the p-GaN region. These holes detrap trapped electrons and prevent against current collapse.
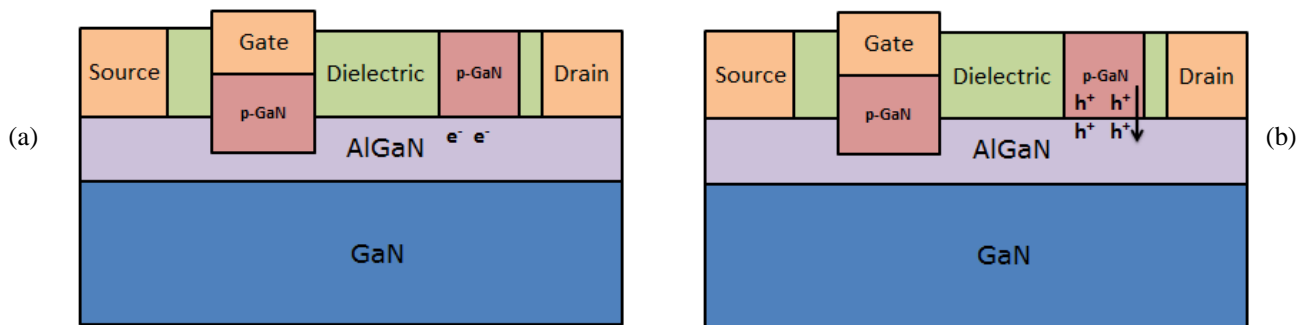
Fig 2-28 The hybrid p-GaN drain for preventing current collapse

2.7.2 The Transphorm Cascode GaN-on-Si HEMT

On the other hand Transphorm have developed a composite GaN-on-Si device. Transphorm have combined a LV E-mode Si MOSFET with a D-mode GaN HEMT to effectively produce an E-mode device [105]. Commercial cascode GaN-on-Si HEMT power devices are of particular interest due to the inclusion of traditional Si FET technology.

In the cascode GaN HEMT device from Transphorm the LV Si MOSFET is connected to the GaN HEMT like so; The Si drain terminal is connected to the GaN source terminal and the Si source terminal is connected to the GaN gate terminal. The Transphorm cascode GaN-on-Si HEMT achieves normally-off operation through this arrangement. This is illustrated in figure 2.29. It is also worth noting that the GaN HEMTs source and gate terminals are inaccessible outside the resin capsule.
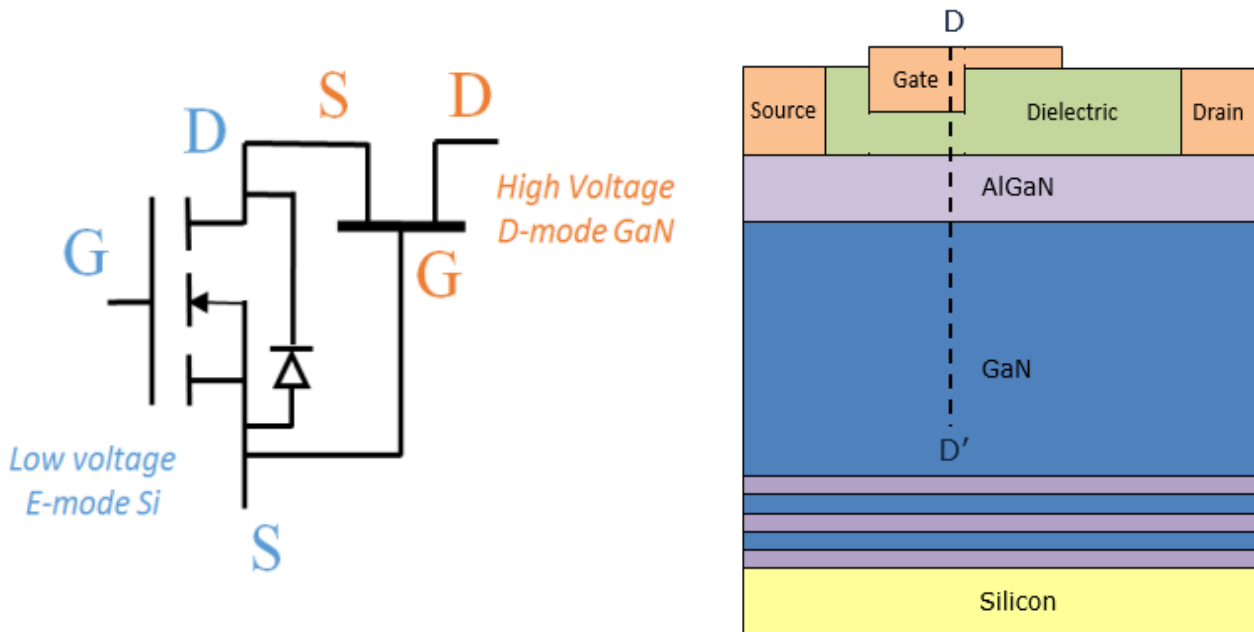
Fig 2-29 A cascode GaN HEMT circuit schematic (left) and structural diagram (right) [106]

In figure 2.30 it is clear that the quantum well is lower than the fermi level and therefore the GaN MISHEMT is normally–on.
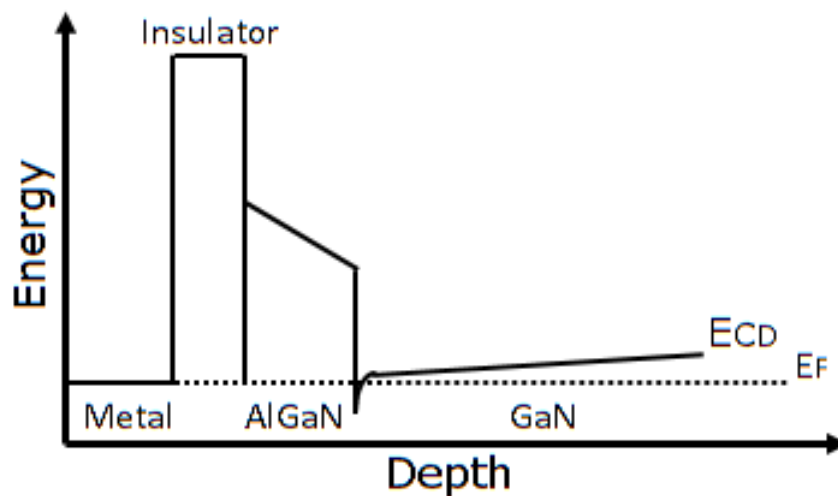
Fig 2-30 The band diagram for the Transphorm GaN MISHEMT

Figure 2.31 displays the GaN-on-Si and Silicon MOSFET die for the Transphorm cascode TPH306PS.
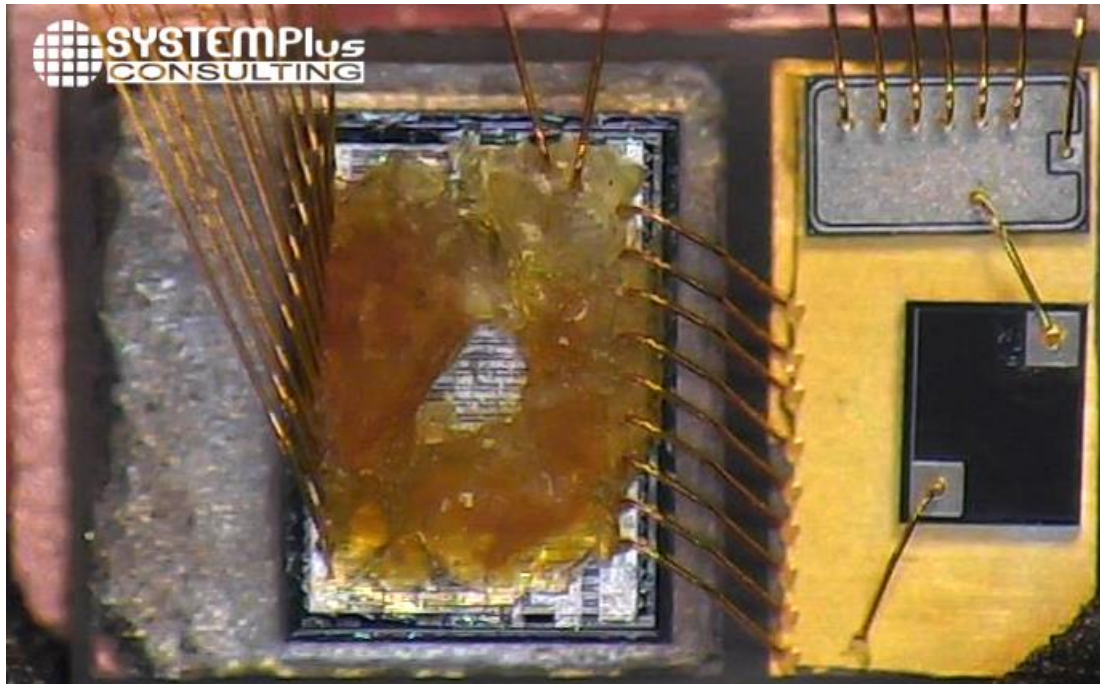
Fig 2-31 The Transphorm cascode TPH306PS GaN-on-Si MISHEMT [107]

As illustrated in figure 2.31 the GaN-on-Si HEMT and the Si MOSFET dies are connected within the capsule. The stray inductance of this package is relatively significant because of the wire joining the two devices.

2.7.2.1 Operation of the cascode GaN-on-Si HEMT

The operation of the Transphorm cascode GaN-on-Si HEMT can be classified into three different categories;

1. Forward Blocking $V_{GS} = 0$, $V_{DS} > 0$.
    A. $0 < V_{DS} < -V_{TH}$ of GaN
    B. $0 < -V_{TH}$ of GaN $< V_{DS}$

2. Forward Conduction $V_{GS} > V_{TH}$ of Si, $V_{DS} > 0$

3. Reverse Conduction
    A. $V_{GS} = 0$
       $V_{GS} > V_{TH}$ of Si
    B. Reverse turn off

[108]

2.8 Summary

This chapter begins by introducing the GaN HEMT and discusses the material and crystal properties of the AlGaN and GaN heterojunction. The atomic properties of Gallium and Nitrogen are presented and the subsequent formation the Wurtzite crystal is explained. The formation and properties of the 2DEG channel in the quantum well has been explained and the normally on operation of GaN HEMT has been stated. The operation and structure of basic and more advance GaN HEMTs have been reviewed. Degradation of GaN devices and reliability issues in GaN-on-Si has been discussed and the addition of surface passivation has been explained. The most prevalent growth techniques have also been discussed with particular focus on the MOVCD technique. The two most promising commercial GaN-on-Si power devices have been discussed. The Cascode GaN-on-Si HEMT has been introduced and their structural, operation and limitations have been discussed. Likewise, the GaN-on-Si GIT has been introduced and their structural, operation and limitations have been discussed.

3 STATIC CHARACTERISTICS OF COMMERCIAL GaN-ON-SI DEVICES AT 300 K

In this chapter, the experimental setup and methodology for the static characterisation of the Si 650 V Infineon SPA15N60C3 Super-Junction (S-J), 600 V Panasonic PGA26C09DV Gate Injected Transistor (GIT) and the 600 V Transphorm cascode TO-220 series devices is presented. The device's I-V, Transfer, R_{ON}, C-V and reverse characteristics are measured and presented. The data is analysed and the performance of each device is critically evaluated against one another. Finally this chapter presents considerations for industrial applications and presents the experiments conclusions.

3.1 Introduction

Although, the performance of cascode HEMTs has been reported in [105], [13], [14] and of p-GaN GIT devices in [103], [101], [110], few works have been produced directly comparing the two, let alone with the state of the art Si technology Therefore, in this paper, we analyse an Infineon Si S-J MOSFET, the Transphorm cascode GaN HEMT and the Panasonic p-GaN layer GaN GIT, providing information on application suitability and evaluating the characteristics of these devices. The remaining parts of this chapter are arranged as follows; in section 3.2, the methodology and experimental setup is defined. In section 3.3 - 3.8, the static characteristics are presented and analysed. Finally, in section 3.10 the conclusions are presented.

3.2 Methodology

The specific models evaluated and compared in this paper are shown in Table 3

Manufacturer	Type of Device	Power Device Model	Rated class	No. of Devices
Transphorm	*Cascode*	*TPH3202PS*	*600V/9A*	*10*
Transphorm	*Cascode*	*TPH3206PD*	*600V/17A*	*10*
Panasonic	*p-GaN*	*PGA26C09DV*	*600V/15A*	*2*
Infineon	*S-J*	*SPA15N60C3*	*650V/15A*	*3*

Tab 4 the devices used in the 300 K static characteristic experiments

3.2.1 Experimental Setup

Devices were measured at a constant temperature of 300 K, using the Keysight B1505A Power Device Analyzer [111] [112]. The devices were inserted into the 500 Amp Ultra-High Current 3-pin inline package socket module on the N1265A Ultra-High Current Expander/Fixture which was connected to the B1505A Power Device Analyzer. For capacitance measurements the N1260, High Voltage Bias was used. Cable parasitics were limited through calibrations and appropriate cable selection. The junction temperature (T_j) of the Device Under Test (DUT) was monitored every 2 seconds using a thermocouple attached to the device's heat sink, applying the assumption that the temperature at the heat sink is the same as the device's T_j. Fig 3 displays the B1505A oscilloscope view. This was used to verify the measurement window (red), pulse period, pulse width, voltage and current. Furthermore, it should be noted that a 100 Ω resistor was connected to the gate to minimize the overshoot oscillations and encourage steady state operation at the measurement window. If not specified, devices were tested using the parameters provided by their respective datasheet [113]–[115]. In addition, throughout the experiments pulsed measurements were used to limit the self-heating effect on the devices.
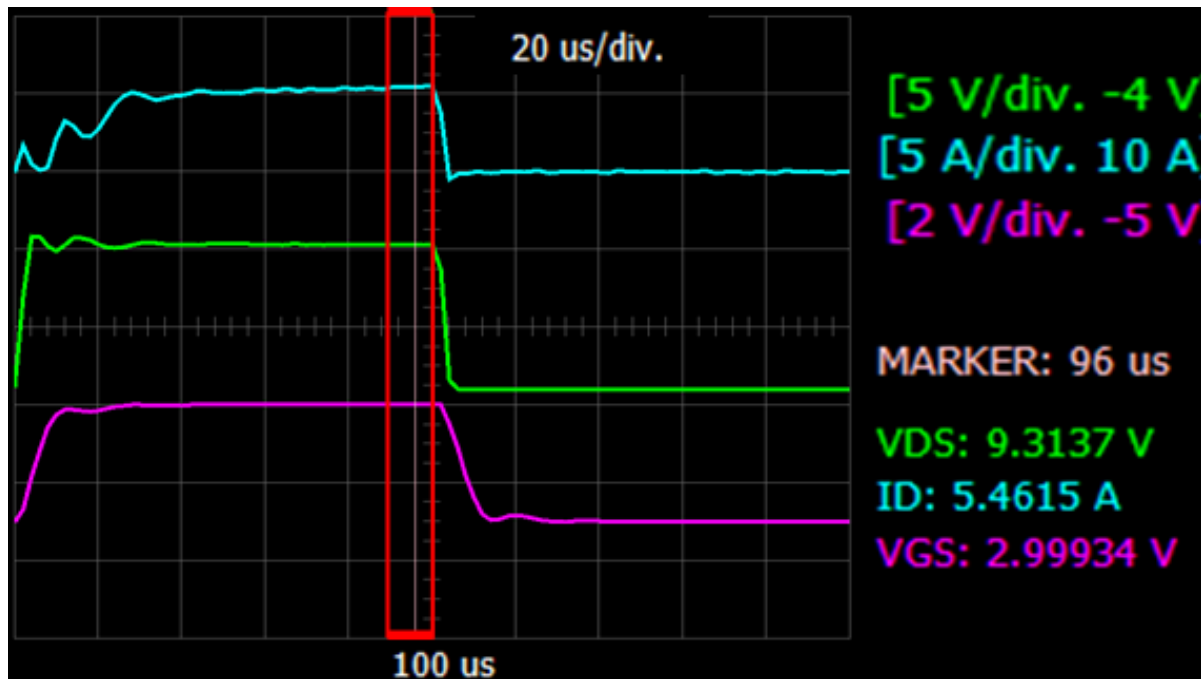
Fig 3-1 Measurement verification using the Keysight B1505A oscilloscope view

Fig 4 displays the Keysight B1505A Power Device Analyzer, the N1265 Ultra-High Current Expander/Fixture, the N1260 High Voltage Bias Tee and the 500 Amp Ultra-High Current 3-pin inline package socket module. With this equipment the forward (I_{ds}-V_{ds}), reverse (I_{ds}-V_{ds}), transfer (I_{ds}-V_{gs}), on-state resistance (R_{ON}), Capacitance-Voltage (C-V) and breakdown voltage (BVDSS) measurements were performed. Throughout the paper, I_{ds} denotes the drain-source current, V_{ds} the drain-source voltage and V_{gs} the gate-source voltage.

Fig 3-2(a) the Keysight B1505A Power Device Analyzer and N1265 Ultra High Current Expander/Fixture. (b) The N1260 High Voltage Bias Tee. (c) The 500 Amp Ultra-High Current 3-Pin Inline Package Socket Module

3.3 Forward I-V Characteristics

Table 4 summarises the parameters used to perform the measurements of the pulsed forward I_{DS}-V_{DS} characteristics.

Device	V_{GS} (V)	Step (mV)	V_{DS} (V)	Step (mV)	Pulse Width (µS)	Pulse Period (S)
SPA15N60C3	0-10	1000	0-10	100	100	1
PGA26C09DV	0-4.5	500	0-10	100	100	1
TPH3202PS	0-10	1000	0-10	100	100	1
TPH3206PD	0-10	1000	0-10	100	100	1

Tab 5 the experimental parameters of forward I-V characteristics

Fig 3.3 displays the pulsed forward (I_{ds}-V_{ds}) *characteristics of the SPA15N60C3 S-J (a), the* PGA26C09DV GIT (b), TPH3202PS (c) and TPH3206PD (d) GaN HEMTs.
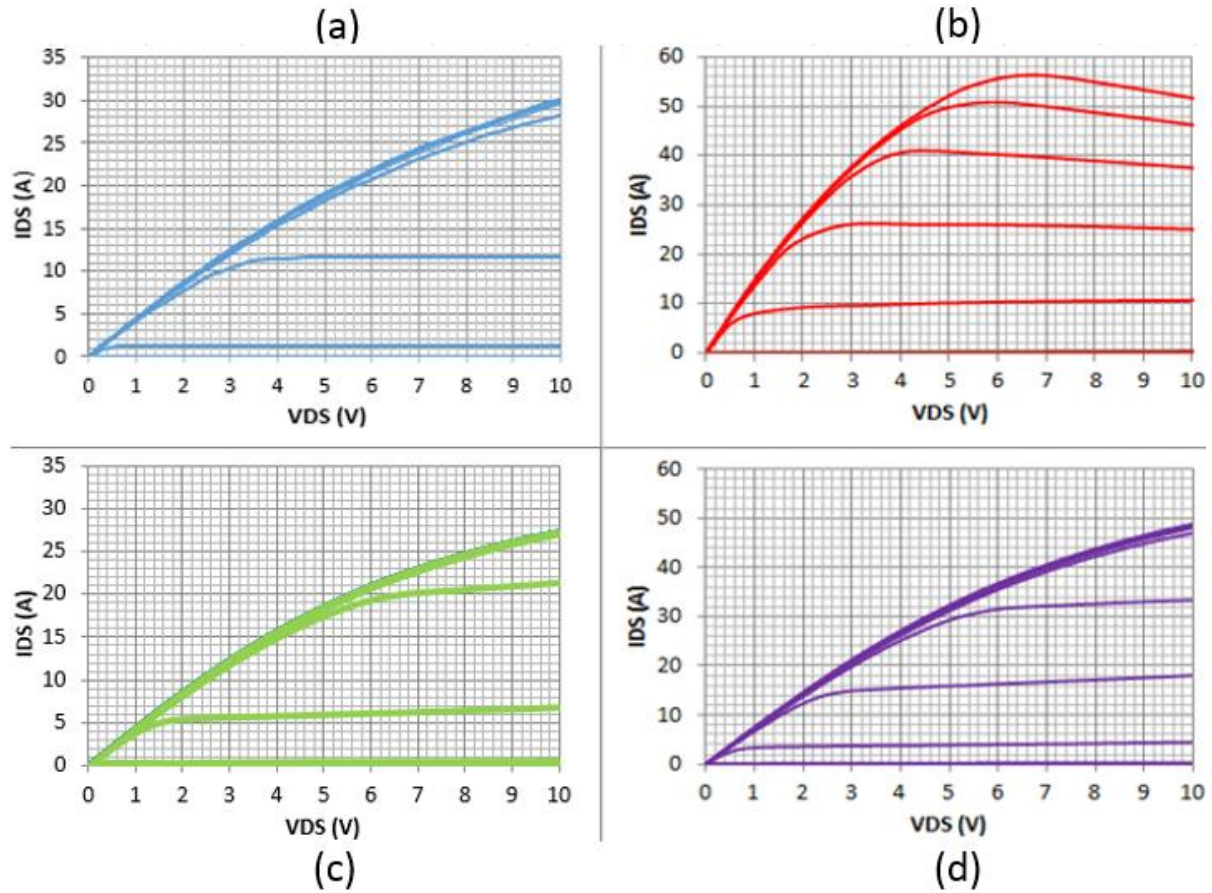
Fig 3-3 Forward I_{DS}-V_{DS} characteristics

The measured I_{ds}-V_{ds} characteristics for the Transphorm TPH3202PS and TPH3206PD display a considerable difference with the manufacturer's datasheet [114], [115]. They experienced a saturation of I_{ds} 44 A at V_{gs} 7 – 10 V. In contrast, the datasheet states that the device should have an I_{ds} of + 80 A for a V_{gs} of 10. The Transphorm TPH3206PD measurements match the experimental and simulated results of [116]. In addition, these agree with the experimental I-V characterisation of a Transphorm TPH3206PD in [117]. The Panasonic PGA26C09DV shows superior I_{ds}-V_{ds} characteristics compared the similarly rated Transphorm TPH3206PD and Si SPA15N60C3 S-J device

3.4 Reverse I-V Characteristics

Table 5 summarises the experimental parameters for the pulsed reverse I_{ds}-V_{ds} characteristics.

Tab 6 the experimental parameters for reverse I_{DS}-V_{DS} characteristics

Device	V_{gs} (V)	Step (mV)	V_{ds} (V)	Step (mV)	Pulse Width (µS)	Pulse Period (S)
SPA15N60C3	0-10	1000	0 to -10	100	100	1
PGA26C09DV	0-4.5	500	0 to -10	100	100	1
TPH3202PS	0-10	1000	0 to -10	100	100	1
TPH3206PD	0-10	1000	0 to -10	100	100	1

Fig 3.4 displays the pulsed reverse (I_{ds}-V_{ds}) characteristics of the SPA15N60C3 S-J (a), the PGA26C09DV GIT (b), TPH3202PS (c) and TPH3206PD (d) GaN HEMTs
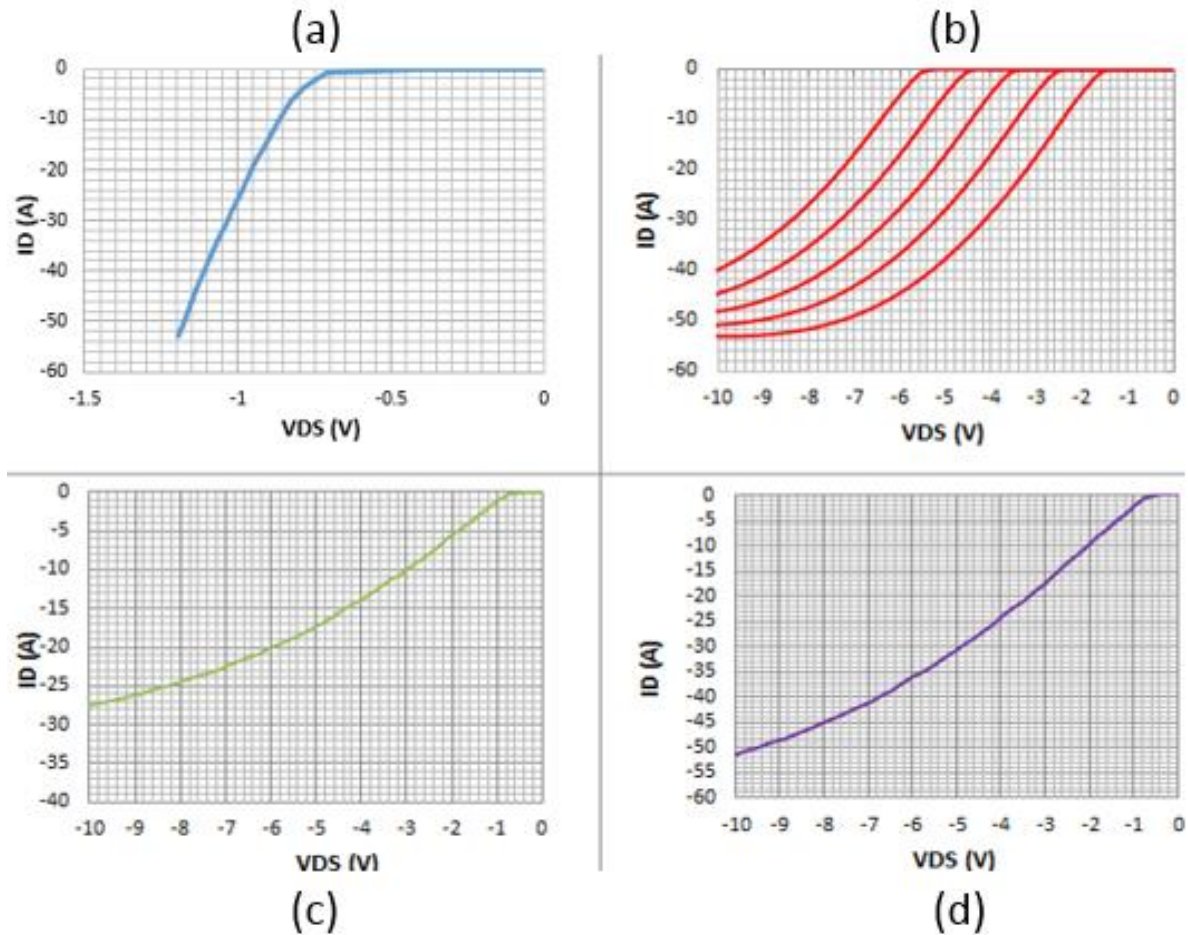
Fig 3-4 Reverse I_{ds}-V_{ds} Characteristics

GaN HEMTs do not have a body diode [99] this is also the case for the Panasonic GIT (see diagram of Fig. 1). With the absence of an anti-parallel body diode, reverse conduction is possible if the drain voltage falls below the sum of the gate potential and the threshold voltage. This method of reverse conduction is reverse-recovery free which makes it ideal for applications like half-bridge and full-bridge converters [118]. In contrast, the Infineon S-J and Transphorm cascode HEMTs have an antiparallel body diode.

3.5 Transfer Characteristics

Table 6 summarises the experimental parameters for the transfer characteristics I_{ds}-V_{gs}.

Device	V_{gs} (V)	Step (mV)	V_{ds} (V)	Pulse Width (µS)	Pulse Period (S)
SPA15N60C3	0-10	1000	10	100	1
PGA26C09DV	0-4.5	500	10	100	1
TPH3202PS	0-10	1000	10	100	1
TPH3206PD	0-10	1000	10	100	1

Tab 7 the experimental parameters of the transfer I_{DS}-V_{GS} measurements

Fig 3.5 displays the pulsed (I_{ds}-V_{gs}) transfer characteristics of the SPA15N60C3 S-J, the PGA26C09DV, the TPH3202PS and TPH3206PD GaN HEMTs.
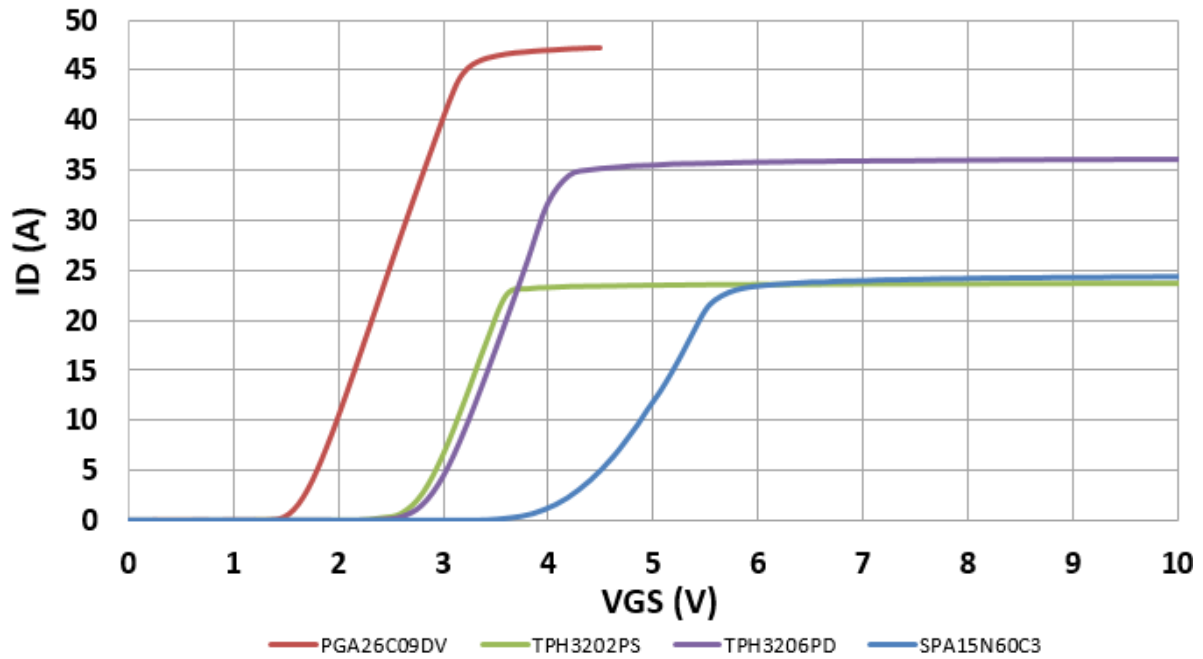
.Fig 3-5 I_{DS}-V_{GS} Transfer Characteristics.

The device threshold voltages (V_{TH}) were obtained using the method of linear extrapolation of I_{ds}-V_{gs} curves [119]. The transfer characteristics corroborate with the typical properties of naturally E-mode HEMT devices with relatively low gate V_{TH} reported by [6]. The Panasonic PGA26C09DV has a gate V_{TH} of 1.2 V compared to the Transphorm TPH302PS and TPH3206PD's 2.5 V_{TH}. This greater V_{TH} can be attributed to Transphorm's use of the cascaded LV Si MOSFET illustrated in Fig 1. The LV Si MOSFET is arranged to drive the GaN device. Therefore, it will determine the overall device's V_{TH}. Contrary to this, the PGA26C09DV is driven solely by the p-gate.

In addition, according to the datasheet, the maximum operation V_{gs} for the Panasonic PGA26C09DV is relatively low at 4.5 V. It has been reported that large gate voltages in GITs by even small amounts may lead to device failure [116]. However, we experimented with gate voltages well above 10 V and found no device failures. On the contrary, Transphorm's TPH3202PS and TPH3206PD devices are capable of withstanding gate voltages up

to 18 V according to their respective datasheets. This is because of the LV Si MOSFET driving the composite device. The higher gate breakdown voltage allows a certain degree of freedom to use traditional Si MOSFET drivers and lessen the complexity of system safeguards to prevent the premature failure of the power device. Furthermore, although temperature has not been considered in these experiments, real application may induce small V_{TH} shifts which can render the device uncontrollable or to behave in a non-desirable manner.

3.6 On Resistance Measurements

Table 7 summarises the experimental parameters for the *pulsed forward R_{on}-I_{ds}* characteristics.

Device	V_{gs} (V)	I_D (A)	Step (mA)	Pulse Width (μS)	Pulse Period (S)
SPA15N60C3	4.5	1-44	100	100	1
PGA26C09DV	2.5	1-45	100	100	1
TPH3202PS	4.5	1-24	100	100	1
TPH3206PD	4.5	1-36	100	100	1

Tab 8 experimental parameters for R_{ON}-I_{DS} characteristics

Fig 3.6 displays the forward pulsed R_{on} vs I_{ds} characteristics of the SPA15N60C3 S-J, the PGA26C09DV, the TPH3202PS and TPH3206PD GaN HEMTs
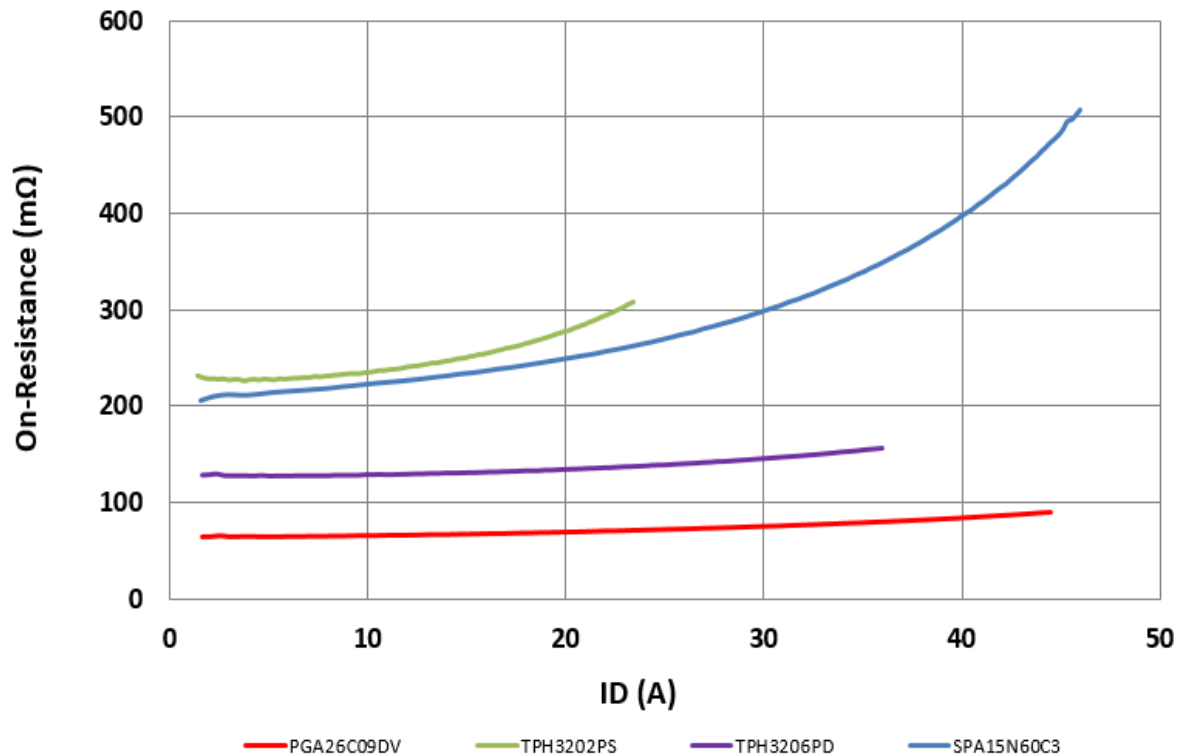
Forward R_{on}-I_{ds} Characteristics

The Panasonic PGA26C09DV has a significantly lower R_{on} than the Transphorm devices. In addition, compared to the state-state-of-the-art Si MOSFET technology the PGA26C09DV has one thirteenth of the On Resistance,

Gate Charge ($R_{on}Q_q$) [120], which is an important for fast switching. The Transphorm devices still display impressive R_{on} values when compared to similarly rated Si technology [102]. Reportedly, 10% of the resistance in the cascode devices can be contributed to LV Si MOSFET to GaN HEMT connection [105]. Recently a wire bond-less package for a cascode GaN HEMT has been presented in [121]. This may further reduce the R_{on} and provide more reliable operation without wire bond lift-off failures and smaller parasitics. However, even with this reduction in parasitics attributed to the LV Si MOSFET to GaN HEMT bond wires, the PGA26C09DV still displays considerably lower R_{on}. Achieving this lower R_{on} has significant impacts in the overall system in terms of efficiency and power loss for power supply system's as reported by [122].

3.7 CV Measurements
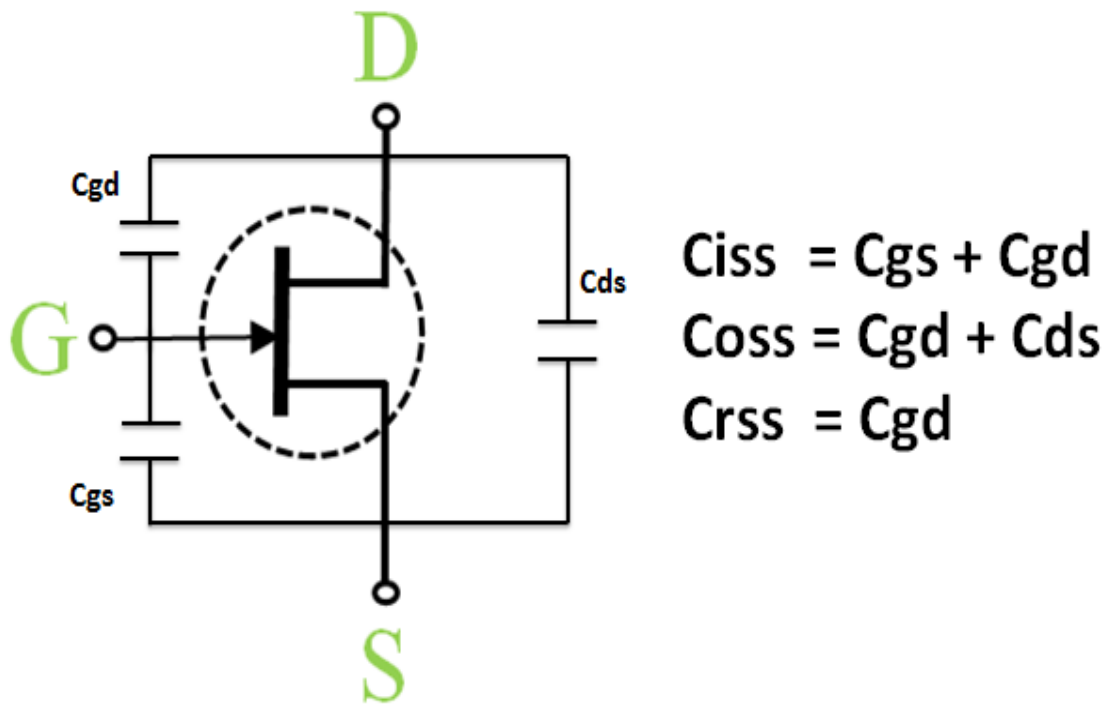
Fig 3-6 Equivalent Capacitance Diagram for the E-mode GaN GIT displaying the Output Capacitance (Coss), Input Capacitance (Ciss) and Reverse Capacitance (Crss) Components

Table 8 summarises the experimental parameters for the C-V measurements.

Device	V_{ds} (V)	Step (V)	Frequency (MHz)
SPA15N60C3	0.1-650	0.65	1
PGA26C09DV	0.1-650	0.65	1
TPH3202PS	0.1-650	0.65	1
TPH3206PD	0.1-650	0.65	1

Tab 9 the experimental parameters for the C-V measurements

Figure 3.7 displays the Coss, Ciss and Crss measurements of the SPA15N60C3 S-J, the PGA26C09DV, the TPH3202PS and TPH3206PD GaN HEMTS.
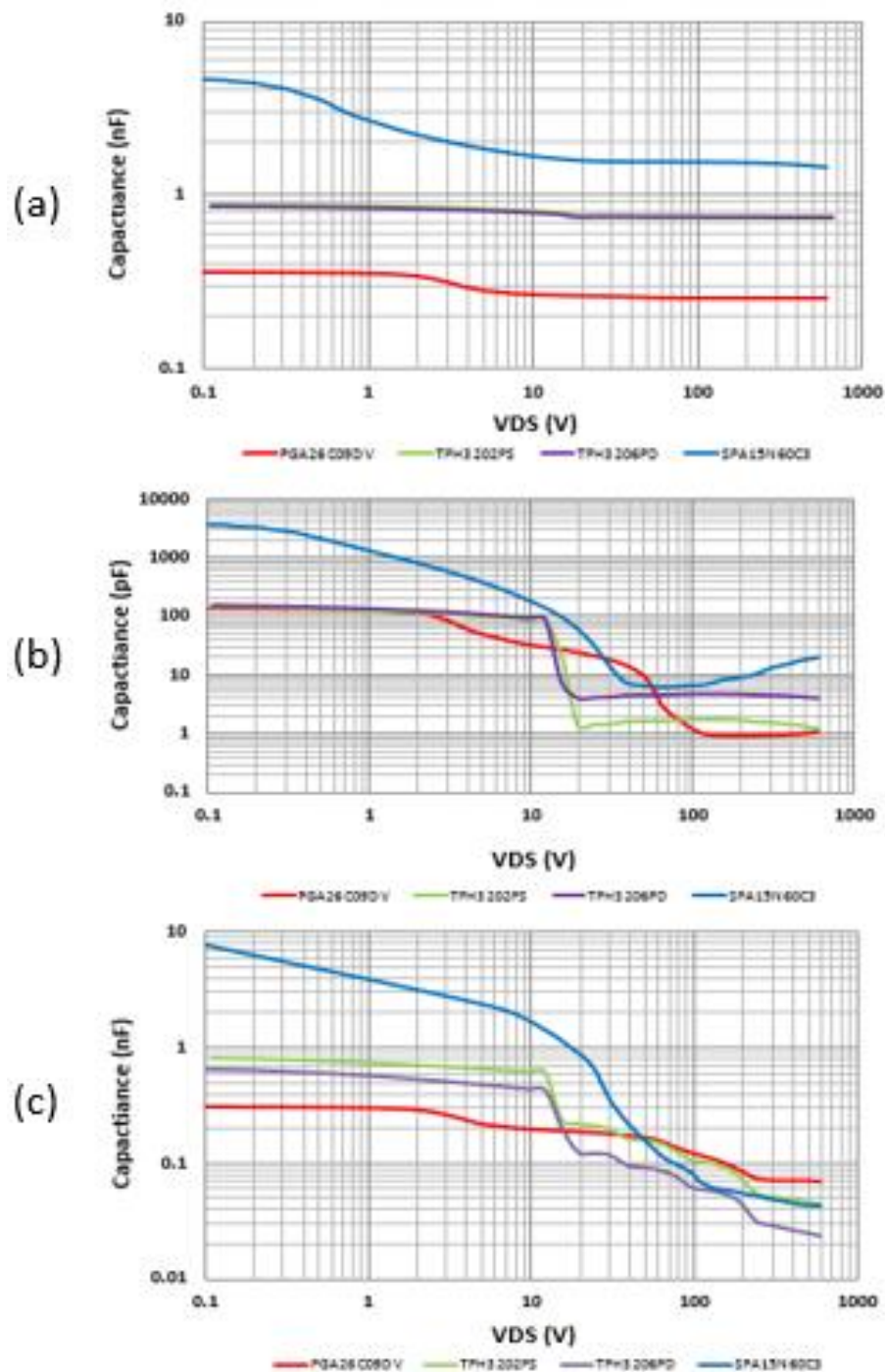
Fig 3-7 The C-V measurements for Coss, Ciss and Crss

The Panasonic PGA26C09DV device has significantly lower Coss, Ciss and Crss values than the two Transphorm devices. This is attributed to the overall design of the device. For switching applications, it is highly desirable to have low Ciss. Turn-on/Turn-off delays are proportional to the devices Ciss, increasing this time will prevent high speed switching capabilities. For the Transphorm cascode device, the Ciss is dominated by the LV Si MOSFET. However, driver loss is less significant for High Voltage (HV) applications. In the cascode devices Coss is dominated by HV Metal Insulated Semiconductor Field Effect Transistors D-(MISFETs), which is promising due

to D-MISFETs intrinsic low output capacitance property [123]. The cascode Gate to Drain Capacitance (Cgd), which determines major switching losses, is mainly composed of HV D-MISFET's the Drain to Source capacitance (Cds), the LV Si FET's Cgd/Coss ratio and Zener diode capacitance. In this case, the HV D-MISFET, LV Si FET and Zener diode need to be carefully designed to achieve an optimized Cgd for the cascode device to ensure high switching capabilities as device size and transconductance play a role in this. It should be noted that we did not measure the gate charge (Qq). The Transphorm TPH3202PS has higher capacitance values than the TPH3206PD device.

3.8 BVDSS Measurements

Table 9 summarises the experimental parameters for the BVDSS measurements

Device	V_{gs} (V)	V_{ds} (V)	Step (V)	Max I_{ds} (µA)
SPA15N60C3	0	0-1000	1	100
PGA26C09DV	0	0-1000	1	100
TPH3202PS	0	0-1000	1	100
TPH3206PD	0	0-1000	1	100

Figure 3.8 displays the BVDSS characteristics of the SPA15N60C3 S-J, the PGA26C09DV, the TPH3202PS and TPH3206PD GaN HEMTs. The measurements shown are for new devices with multiple devices tested. All these waveform experience some level of noise contributed by the limitations of the measurement equipment.
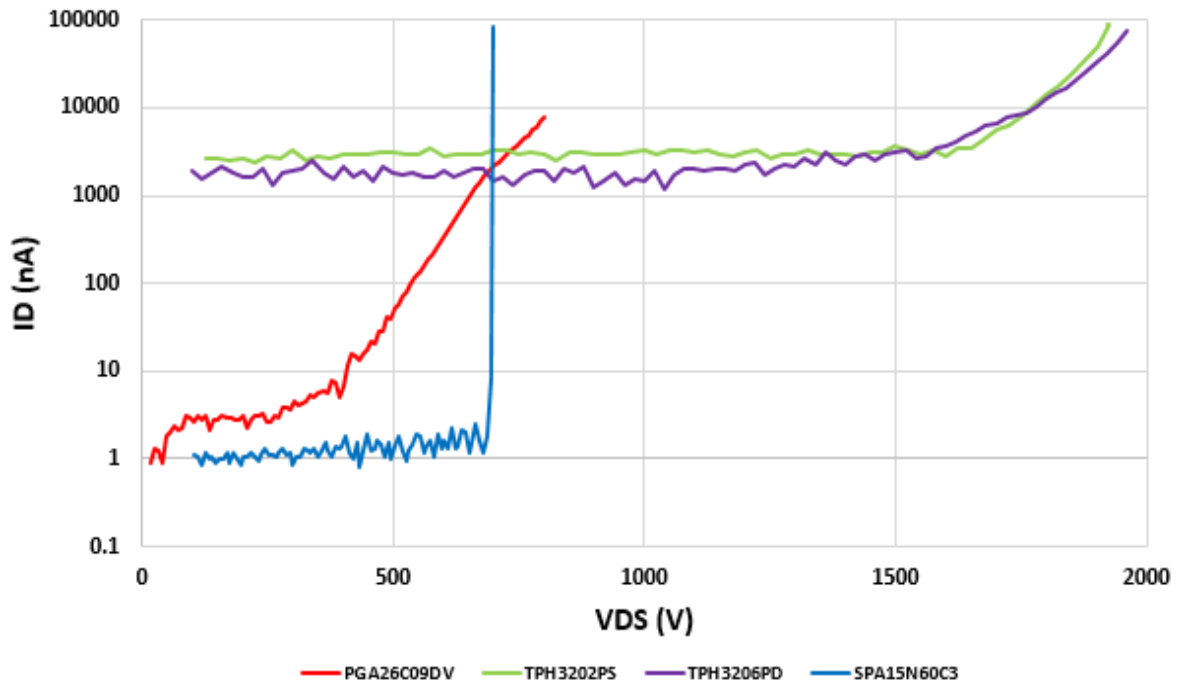
Fig 3-8 BVDSS measurements

The Panasonic PGA26C09DV GIT has a drain leakage current a magnitude lower than the Transphorm devices and a breakdown voltage of approximately 750 V. Both Transphorm devices display similar drain leakage currents and breakdown voltages in the region of 1850 V. GaN has a critical electric field of 3.3 MV [89]. This high critical electric field allows large avalanche breakdown voltages.

Each of the Transphorm devices tested had over a 250% greater breakdown voltage than the maximum V_{DS} value. The reason for this is in HEMT devices it is not the semiconductor that limits the voltage blocking capability. Indeed, HEMT devices do not fail by avalanche induced breakdown. Instead, they primarily fail because of Time Dependent Dielectric Breakdown (TDDB) [124]. Therefore, Transphorm have designed these devices to withstand three times the amount of rated V_{ds} so to ensure that premature device failures because of dielectric breakdown will not occur under normal operating conditions [125]. However, motivation for this over-engineering may possibly be the need to pass the reliability tests.

3.9 Further Considerations for Industrial Applications

The Si S-J has been proven to be reliable, cost effective and efficient. This has yet to be confirmed for WBG devices. In addition, WBG devices experience different failure modes in comparison to Silicon ones. Current reliability validation is performed through avalanche specific tests. As mentioned before, GaN devices experience dielectric breakdown. Therefore, application relevant testing approaches have been suggested by [126] to provide greater indications of device performance. That being said, the static characterization that is reported in this paper provides an indication about how the performance of the devices and how technologies compare. It also highlights potential issues and limitations. Understanding and determining those performance limits, is essential for the design of efficient and reliable converters.

Due to the characteristics of E-mode GaN HEMTs, specialized gate drivers and careful drive techniques need to be utilized when they are included in a system. As of yet these specialized gate drivers have not been proven to be reliable. Texas Instrument's LM5114 gate driver is designed to drive individual GaN devices but it cannot provide signal isolation [127]. Fig 13 displays the topology for a simple boost converter using a LM5114 Single 7.6-A peak current low-side gate driver. The GIT device is highly susceptible to the noise induced by the system's parasitics. The consequences of this scenario may produce catastrophic results unless steps are taken to minimize the effect of this parasitic interference. For example, efficient design for the PCB layout can be performed in which the inductance and distance between the GIT and the driver is minimal.
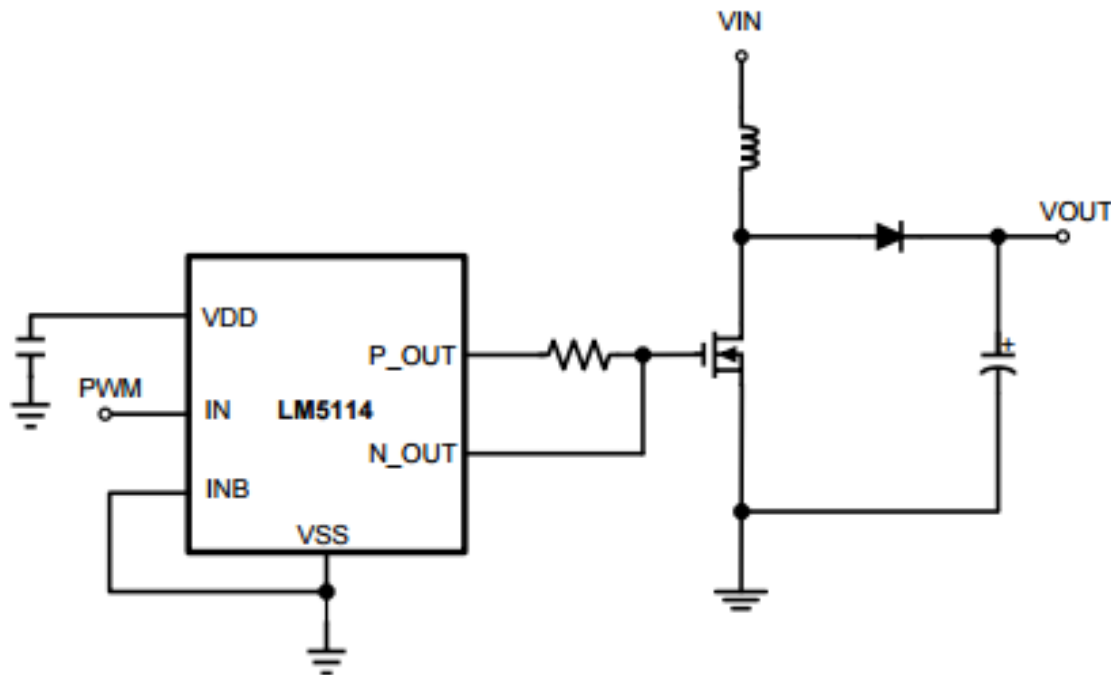
Fig 3-9 Topology For a Simple Boost Converter Using an LM5114 Single 7.6-A Peak Current Low-Side Gate Driver [128]

In contrast, D-mode GaN cascode HEMTs do not need specialized gate drivers because they are driven by traditional Si FET technology. However, although the GaN cascode HEMT only requires traditional Si gate drivers the device experiences insufficient slew control. In addition, the LV Si MOSFET faces avalanche failure due to the static voltage sharing [129]. Low avalanching voltages could be solved by replacing the LV Si MOSFET

with a HV Si MOSFET. However, a HV Si MOSFET would increase the specific R_{on}-I_{ds} for the device and increase the power loss of this device. In addition, would require the GaN's gate-source capabilities to be raised accordingly.

Also it should be noted that due to the high frequency capabilities of GaN devices and large stray inductance present in the package of GaN devices, there is extreme challenge in the optimal package configuration. These stray inductances in traditional device packages such as the TO-220 have prevented the exploitation of the full switching capability of GaN devices. The stray inductances also increase the losses in dynamic operations because of the increased switching times [130].

Therefore, GaN device manufacturers are packaging GaN-on-Si in low inductance or optimized package configurations. Transphorm have taken special consideration in designing devices with effective terminal configurations. For TO-220 packages the terminal layout is Gate-Source-Drain (GSD) as opposed to the conventional Gate-Drain-Source (GDS) power terminal layout. The terminal configuration is designed to minimize the Gate-Source driving loop parasitic inductance and to isolate the driving loop from the power loop, minimizing noise [131].

3.10 Summary

In this work, the static performance at 300 K of commercial GaN-on-Si devices was determined experimentally. Two different GaN-on-Si technologies, the E-mode GIT from Panasonic and D-mode cascaded HEMT from Transphorm, were characterized and benchmarked against a Si S-J MOSFET.
Experimental results in this paper have demonstrated a high variation in the performance of the Transphorm devices compared to their respective datasheets. Further, the Transphorm devices did not break until about 1850 V, despite being rated at 600 V. This corresponds to approximately 250% over-engineering on this device's maximum voltage rating.

Comparing the GaN-on-Si devices, the Panasonic PGA26C09DV has a lower leakage current for voltages up to 600V, where the breakdown was observed as expected. The C-V measurements indicated that the Panasonic device is faster, which can be expected, being a purely GaN based device compared to the cascade configuration. The Panasonic GIT also featured a lower R_{ON} too. However, the Transform device has a higher threshold voltage, which is desirable. In relation to the Si S-J, both GaN-on-Si technologies displayed impressive results. The GaN GIT device, outperformed the Si S-J in terms of R_{ON} and displayed interesting I-V characteristics. The two Transphorm devices also performed respectively well, with the TPH3206PD displaying similar R_{ON} values. The Si S-J displayed lower leakage currents than the both the GaN-on-Si technologies at 300 K. This however, may change with higher operation temperatures, as GaN has a wider band gap energy. High temperature static measurements will therefore, be need to assess the performance of these devices.

Each device presents unique advantages that suit different applications. It can be concluded that the Panasonic device is more suited to applications where switching and efficiency are high priorities. On the other hand, Transphorm devices suit applications where spike voltages and greater gate control is desired. It should also be stated that although GaN-on-Si offers unmatched performance capabilities, modern Si S-J MOSFETs are still competitive and capable of outperforming GaN technology in certain properties.

4 CONCLUSIONS AND FUTURE WORK

4.1 Conclusions of this Research

In this thesis the fundamental theory behind GaN HEMTs has been discussed with particular focuses on the crystal lattice, operation and structural properties of these devices. A literature review has been performed that develops on the heterojunction interface between the AlGaN and GaN layers. Chapter 3 has demonstrated that GaN-on-Si devices have demonstrated a good level of performance in the static characterisation experiment performed at 300 K. However, Si super junction technology is still competitive and displays superior off state leakage currents. The Panasonic GaN-on-Si GIT displays low on state resistance due to the conductivity modulation presented in chapter 2. As literature suggested the GaN-on-Si cascode HEMT displayed robust performance and underwent dielectric breakdown at approximately 1850 V.

4.2 Future Work

It is important to acknowledge that the analysis and understanding of device performance is a continually developing field. The development of electronic devices is a fast moving and continually changing environment and therefore, so is the field of performance and reliability indication. Additional research in this area should focus on the diverse and extensive list of specific laboratory applications for power devices; however, their performance cannot be comprehensively measured effectively with a limited number of laboratory experiments. In fact, the best and only true test of the performance and reliability of any power device is their introduction into industrial applications. Having stated this: further laboratory transient experiments should be performed which focus specifically on the potential power losses of switches and also; soft and hard switching operations. In addition, transient experiments with temperature variations would be extremely useful for determining the performance of power switches in "real world" operations.

Another aspect requiring further investigation of, is the development of relevant reliability experiments. Traditional reliability experiments including the well-known JEDEC qualifications, HTRB, HVOS and HVGS should be performed to indicate and project the long term reliability of these devices. However, it is well documented that the validity of conventional reliability and lifetime experiments has been questioned, therefore the development of effective testing is important. Progression in this area should pay close attention the JC-70 committee which has recently been formed to address the introduction of WBG materials into the field of power electronics.

The inclusion in future testing of SiC based power devices would be significantly beneficial for comparisons of performance and reliability in different technologies. This proposal is even made more attractive with the imminent arrival of 3-SiC based power devices. 3-C-SiC devices offer the same economic benefits as GaN-on-Si due to their ability to be grown on Silicon substrates. As WBG materials become more mature and begin to dominate the commercial market place it is predicted that GaN and SiC will compete in the low to mid voltage and frequency applications. The critical evaluation and comparison on the performance of these devices is, therefore, of real interest.

Finally, the development of TCAD model simulations alongside the additional experiments should be made. The theoretical element of these simulations would provide a strong basis of the performance of actual power devices and ultimately may aid in the development of superior devices.

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APPENDIX A

Parameters	Symbol	Unit	Si	GaAs	AlN	InN	GaN	SiC	Diamond
Crystal structure	–	–	Diamond	Zincblend	Wurtzite	Wurtzite	Hexagonal, cubic	Hexagonal, cubic	Diamond
Density	–	g/cm^3	2.328	5.32	3.26	6.81	6.1	3.21	3.515
Mole	–	g/mol	28.086	144.64	40.9882	128.83	83.73	40.097	12.011
Atomic density	–	atom/cm^3	5.00E+22	4.42E+22	4.79E+22	3.18E+22	4.37E+22	4.80E+22	1.76E+23
Lattice constant	–	Å	5.43095	5.6533	3.1114/a, 4.9792/c	3.544/a, 5.718/c	Hex 3.189/a, 5.185/c, cubic 4.52	(6H)3.086/a, 15.117/c, (4H) 3.073/a, 10.053/c, (3C) 4.3596/a, 3.073/c	3.567
Melting point	–	°C	1415	1238	2200	1100	2573, @60 kbar	2830	4373, @125 kbar
Specific heat	–	J(g °C)	0.7	0.35	0.748	0.296	0.431	0.2	0.52
Linear thermal expansion coefficient	–	°C^{-1}	2.60E−06	6.90E−06	5.27E−6/a 4.15E−6/c	3.8E−6/a 2.9E−6/c	5.6E−6/a 3.2E−6/c	~5E−6	8.00E−07
Thermal conductivity	–	W/(cm °C)	1.5	0.46	2.85		2.1	2.3–4.9	6–20
Transition type	–	–	Indirect	Direct	Direct	Direct	Direct	Indirect	Indirect
Bandgap energy	Eg	eV	1.12	1.42	6.2	0.65	3.39(H)	3.02/6H 3.26/4H 2.403/3C	5.46–5.6
Separation energy	Γ-L, Γ-X	eV	Indirect	Γ-L0.29, Γ-X0.48s	Γ-ML 0.7 Γ-K 1.0	Γ-A > 0.7 Γ-Γ > 1.1 Γ-K > 2.7	Γ-Γ'1.9 Γ-M 2.1	Indirect	Indirect

Tab A. Material properties of significant power semiconductors [16]

Parameters	Symbol	Unit	Si	GaAs	AlN	InN	GaN	SiC	Diamond
Dielectric constant	ε_r	–	11.7	12.9, 10.89@RF	8.5	15.3	12	10.0(6H) 9.7(4H)	5.7
Electron affinity	χ	eV	4.05	4.07	1.9	5.8	3.4	4	(NEA)
Intrinsic carrier density	n_i	cm^{-3}	1.45E+10	1.79E+06	9.40E−34	9.20E+02	1.67E−10	1.16E−8(6H) 6.54E−7(4H)	1.00E−26
Effective density of states	N_c	cm^{-3}	2.80E+19	4.70E+17	4.10E+18	1.30E+18	2.24E+18	4.55E+19(6H) 1.35E+19(4H) 1.53E+19(3C)	1.00E+20
Effective density of states	N_V	cm^{-3}	1.04E+19	7.00E+18	2.84E+20	5.30E+19	1.16E+19	1.79E+19	1.00E+19
Effective mass	$m*_e$	$m*el/m_0$ $m*et/m_0$	0.9163/l, 0.1905/t	0.067	0.4	0.1–0.05	0.2	1.5/l, 0.25/t	1.4/l, 0.36/t
Effective mass	$m*_h$	$m*lh/m_0$ $m*hh/m_0$	0.16/l, 0.49/h	0.082/l, 0.45/h	0.6	1.65	0.6/h	0.8	0.7/l, 2.1/h
Electron mobility	μ_e	$cm^2/(V\ s)$	1500	8500	300	3200	1000	460–980	2200
Hole mobility	μ_h	$cm^2/(V\ s)$	450	400	14	220	~5	20	1800
Lattice matching	–	–	~SiGe	AlAs, InGaP	~GaN	–	~SiC, sapphire	~GaN, lN	–

10 Material properties of significant power semiconductors extended [16]

Manufacturer	Product No	Technology	Package	Release	Current (A)	Min VDS (V)	Max R_{ON} (mΩ)	Supplier	Cost £
EPC	EPC2012C	eGaN FET	LGA 1.7 x 0.9	2014	5	200	100	Digi-Key	2.31
	EPC2019		LGA 2.77 x 0.95	2015	8.5		50		3.09
	EPC2046		BGA 2.77 x 0.95	2017	11		25		5.85
	EPC2010C		LGA 3.6 x 1.6	2015	22		25		5.51
	EPC2047		BGA 4.6 x 1.6	2017	32		10		9.72
	EPC2034		BGA 4.6 x 2.6	2016	48		10		7.09
	EPC2027			2015	4	450	400	N/A	N/A
GaNsystems	GS66502B	eGaN FET	GaN$_{PX}$® 5.0 x 6.6 x 0.51		7.5	650	260	Mouser	8.47
	GS66504B		GaN$_{PX}$® 5.0 x 6.6 x 0.51		15		130		10.99
	GS66506T		GaN$_{PX}$® .6 x 4.5 x 0.54		22.5		90		15.54
	GS66508B		GaN$_{PX}$® 7.0 x 8.4 x 0.51		30		63		15.39
	GS66508P		GaN$_{PX}$® 10.0 x 8.7 x 0.51		30		63		21.24
	GS66508T		GaN$_{PX}$® 6.9 x 4.5 x 0.54		30		63		14.72
	GS66516T		GaN$_{PX}$® 9.0 x 7.6 x 0.54		60		32		49.60

	GS66516B		GaN$_{PX}$® 11.0 x 9.0 x 0.51		60		32		39.06
micro GaN GmbH	MGG1T0617D-CA	SiGaN Diode	TO-220		4	600			
	MGG1T0617D	dGaN HEMT	TO-220	2012	30		210		
			Bare Die						
	MGG1T0617D-CO	Cascode	TO-220				320		
ON-Semiconductor‡	NTP8G202NG	Cascode	TO-220	2015	9	600	350	Mouser	16.07
	NTP8G206NG				17		180		21.78
Panasonic	PGA26C09DV*	GIT	TO-220	2015	15	600	71	Mouser	N/A
	PGA26E19BA		DFN	2014	13		190		14.00
	PGA26E07BA		DFN	2016	26		70		27.11
	TPD3215M		HALF-BRIDGE MODULE	2016	70	600	34	Digi-Key	196.71
	TPH3207WS		TO-247	2016	50	650	41		31.46
	TPH3205WSB		TO-247	2017	35	650	60		23.01
	TPH3205WSBQA		TO-247	2017	35	650	62		25.32
	TPH3212PS		TO-220	2016	27	650	85		16.70

Transphorm†	TPH3208PS	Cascode	TO-220	2016	20	650	130		11.88
	TPH3208LD		PQFN88	2016	20	650	130		13.09
	TPH3208LDG		PQFN88	2016	20	650	130		13.09
	TPH3208LS		PQFN88	2016	20	650	130		13.09
	TPH3206PD		TO-220	2015	17	600	180		12.87
	TPH3206LDB		PQFN88	2017	16	650	180		12.10
	TPH3206LSB		PQFN88	2017	16	650	180	Digi-Key	12.10
	TPH3206LDGB		PQFN88	2017	16	650	180		12.10
	TPH3206PSB		TO-220	2017	16	650	180		10.89
Transphorm†	TPH3202PD	Cascode	TO-220	2015	9	600	350		10.56
	TPH3202PS		TO-220	2015	9	600	350		10.56
	TPH3202LD		PQFN88	2017	9	600	350		11.11
	TPH3202LS		PQFN88	2017	9	600	350		11.11

11.Tab Current commercially available GaN-on-Si devices