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# 4.5kV Bi-mode Gate Commutated Thyristor design with High Power Technology and shallow diode-anode

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**Abstract**— The Bi-mode Gate Commutated Thyristor (BGCT) is a reverse conducting Gate Commutated Thyristor (GCT) where the diode regions are intertwined with GCT parts. In this work we examine the impact of shallow diode-anodes on the operation of the GCT and propose the introduction of optimised High Power Technology (HPT+) in the GCT part. In order to assess and compare the new designs with the conventional, a multi-cell mixed mode model for large area device modelling was used. The analysis of the simulation results show that the shallow diode does not affect the MCC whereas the introduction of the HPT+ allows for a step improvement.

## I. INTRODUCTION

The Integrated Gate Commutated Thyristor (IGCT) is the device of choice for high power applications such as medium voltage drives, pumped hydro, STATCOMs, railway interties and power quality applications[1], [2]. The Bi-mode Gate Commutated Thyristor (BGCT) is an advanced type of reverse conducting IGCT (Integrated Gate Commutated Thyristor) with superior device characteristics [3], [4]. It was experimentally verified on 38 mm wafers, 4.5 kV prototypes [4], the design requirements for higher current controllability were analysed in [5] and a novel BGCT design concept that maximises the controllable current while minimises the on state losses was introduced in [6]. The top side of a recently fabricated 91mm BGCT device is shown in Figure 1.

A shallower and lowly doped diode-anode makes local lifetime control redundant because the injection efficiency and recombination can be controlled by adjusting the diode-anode profile which improves the reverse recovery when operating in diode mode [4]. Nevertheless, its impact on current controllability when operating in GCT mode has not been examined. In this work we assess the impact of shallow diode-

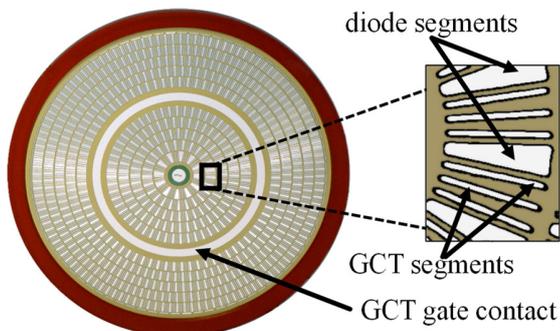


Figure 1. The 91mm, 4.5kV BGCT fabricated prototype.

anodes in the operation of the GCT and propose the introduction of optimised High Power Technology [7], [8] (HPT+) in the GCT part. With the aid of a complex simulation model which was previously calibrated, we performed failure analysis to demonstrate that the proposed BGCT with shallow anode in the diode part and High Power Technology in the GCT part receives a step improvement in Maximum Controllable Current (MCC), a necessary requirement in devices aimed for high power applications.

## II. MODELLING THE BI-MODE GATE COMMUTATED THYRISTOR

Large area (full wafer) devices of the thyristor family are prone to large current redistribution during the turn off process. Studies on GCTs have shown that this is due to parasitic gate inductances within the wafer being non-uniformly distributed [7], [9], [10]. Therefore, in order to reproduce the behaviour of the BGCT in dynamic conditions and in particular to assess full wafer devices in terms of the MCC, the interaction between adjoining regions in the wafer as a result to this imbalance in the gate impedance has to be taken into account. For this a number of two dimensional and three dimensional models have been proposed [5], [11]–[13].

Figure 2 depicts the model used in this work. It was developed for BGCTs in [5] and allows to directly compare the new design with its state-of-the-art conventional counterpart. It accounts for current redistribution in the wafer device during

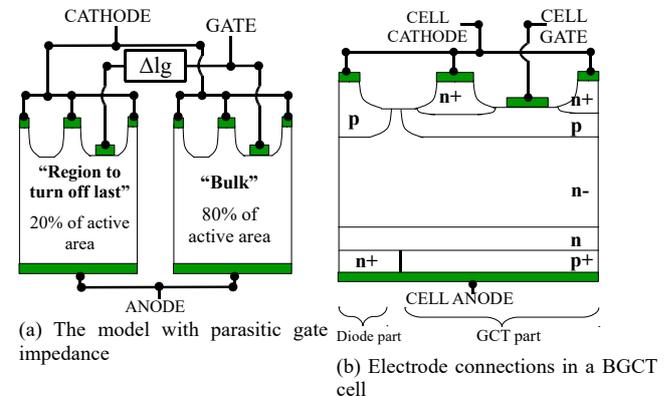


Figure 2. 2D Model for BGCT wafer level simulations.[5]

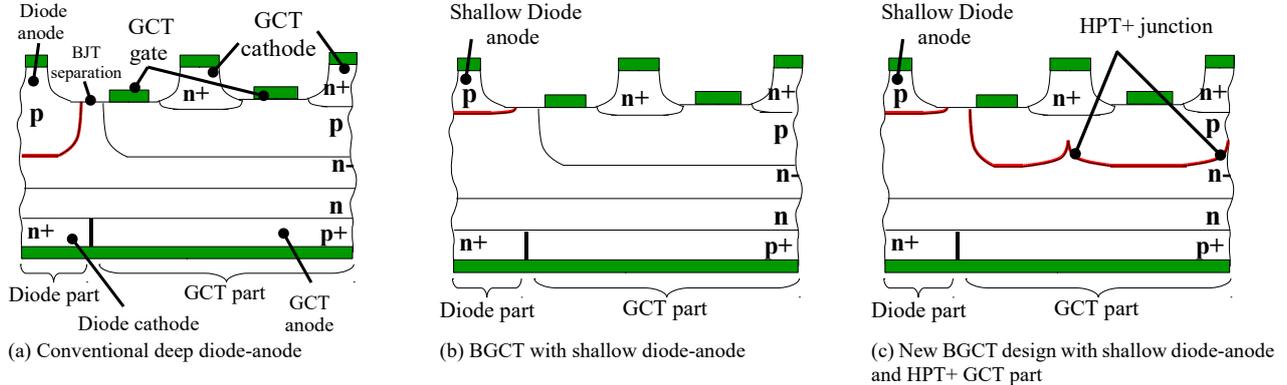


Figure 3: Schematic structure. (a) BGCT with conventional diode-anode. (b) BGCT design with new shallow diode-anode. (c) New HPT+ BGCT with shallow diode-anode.

turn-off due to parasitic uneven gate inductive loading and it can successfully capture via TCAD simulations the overall performance of the BGCT including the failure and the Maximum Controllable Current during inductive switching. In this model, a BGCT wafer device consists of two Finite Element Method (FEM) BGCT cells which are interconnected with wires defined using a compact model. They represent two regions that can be distinguished in a wafer device in terms of how fast they switch off, specifically the “region that turns off last” and the “bulk” of the device. The “region that turns off last” experiences an increased gate inductance and therefore a delayed turn-off signal. Both FEM cells feature an identical doping profile but are scaled up to make up for the approximate area of the equivalent wafer region that they represent. A total active area of  $40\text{cm}^2$  is assumed.

### III. BGCT CELL DESIGN

The conventional reverse conducting IGCT also referred as the RC-IGCT features one single diode region with its anode typically made identical with the p-base of the GCT part, i.e. deep. In the BGCT way of integrating diodes and GCT parts, there is an extra degree of freedom with regards to the diode anode. Indeed, it can be made shallow and even lowly doped to improve the reverse recovery when operating in diode mode. In this work three BGCT variants are considered and analysed. The device schematics are shown in Figure 3:

- BGCT with deep diode
- BGCT with shallow diode anode
- BGCT that maintains the shallow diode anode but also includes an optimised High Performance Technology (HPT+) structured GCT p-base junction.

High Performance Technology has been proved effective in lifting the Maximum Controllable Current (MCC) in IGCTs [7], [8], [14], it is therefore desirable to examine the possibility of including it in the BGCT.

### IV. METHODOLOGY

Current controllability simulation studies have a considerably larger footprint in computational resources when compared to single cell single turn-off simulations. This is because the required mixed mode models include multiple cells and compact circuit components but also because for the determination of the MCC several turn-off simulations are required. The latter is because one simulation can only predict whether the device is able to switch off or not. Every successful turn-off is followed by another turn-off simulation with increased current until a failure is recorded. The conditions for considering a turn-off to be successful are those described in [5]:

**Successful turn-off:** A turn-off is considered to be successful when the anode current reduces to the blocking leakage value right after the tail phase.

**Failure to turn-off:** The GCT is considered to have failed to turn off when during the anode voltage rise period one or more cathode fingers start conducting more than 30% of the on-state anode current value.

### V. RESULTS AND DISCUSSION

The MCC capability of a 4.5kV BGCT with shallow-anode (Figure 3b) is compared with its conventional counterpart (Figure 3a) and the design that incorporates a shallow diode-anode and an optimised High Power Technology junction (HPT+) in the GCT part (Figure 3c). The conclusive MCC results are depicted in Figure 4. Figure 6 depicts the current density contours and electric field just before the failure, and just after. Figure 5 depicts the turn-off failure waveforms for the two BGCT design variants with shallow diode-anode.

#### *BGCT with shallow diode-anode*

As shown in Figure 4, the introduction of a shallow diode-anode in the BGCT does not have a negative impact on the current controllability of the GCT part. This is because the enhanced second peak electric field (Figure 6b) due to the p-regions/n-drift junction depths mismatch is engineered to appear nearer to a gate rather than a cathode.

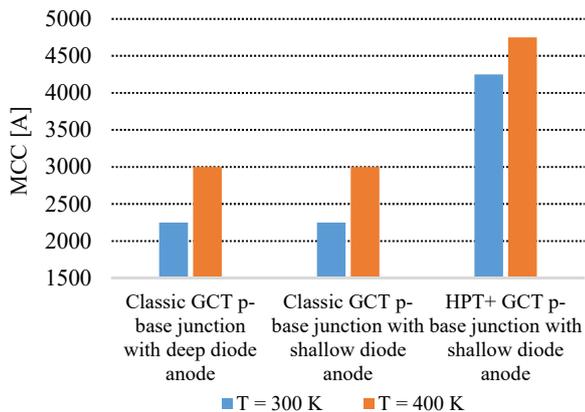


Figure 4: MCC capability of BGCT designs at T = 300 K and T = 400 K, Vdc = 2.7 kV.

### BGCT with shallow diode-anode and HPT+

By introducing the HPT+ structured p-base junction in the GCT part, the current controllability increases substantially. In particular, the **improvement is up to 47% at room temperature and 58% at 400K.**

The peak electric field in BGCTs with standard p-base junction is located right underneath the central cathode segment of the GCT part, the consequent current redistribution due to the local carriers' generation by dynamic avalanche parasitically latches one of the GCT cathodes which enforces the failure (Figure 6c). The structured junction in the HPT+ design "contains" the peak electric field and hence the location of strong dynamic avalanche carriers' generation in regions located underneath the gate rather than the cathode electrode. Therefore, the HPT+ design manages to suppress the adverse

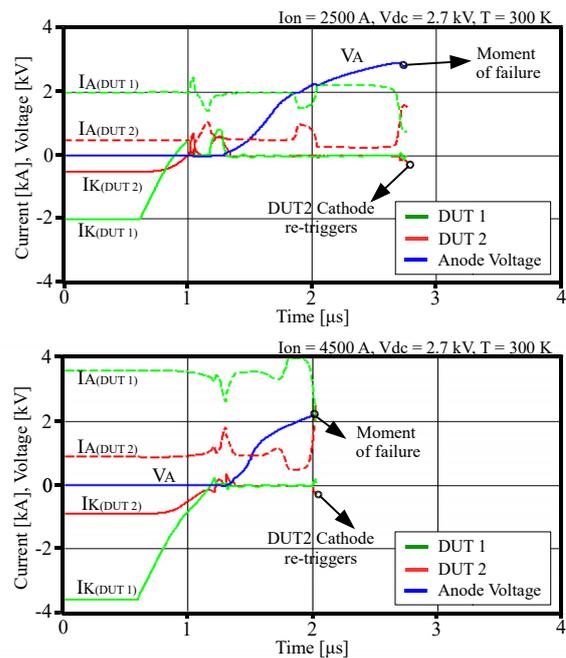


Figure 5: Turn-off failure waveforms for a BGCT design with shallow diode-anode (top) and the new BGCT design with shallow diode-anode and HPT+ GCT part (bottom). "DUT1" refers to "Bulk" region and "DUT2" refers to "region to turn off last" depicted in Figure 2.

effects of dynamic avalanche up to a much higher current level.

### Failure analysis

The failure mechanism is identical for all BGCT designs (dynamic avalanche induced retriggering) but it occurs at a much higher current level when the HPT+ GCT p-base junction is introduced. At the instance prior the failure (depicted in Figure 5), the devices support voltage in excess of 2000 V while still conducting the full load current. The

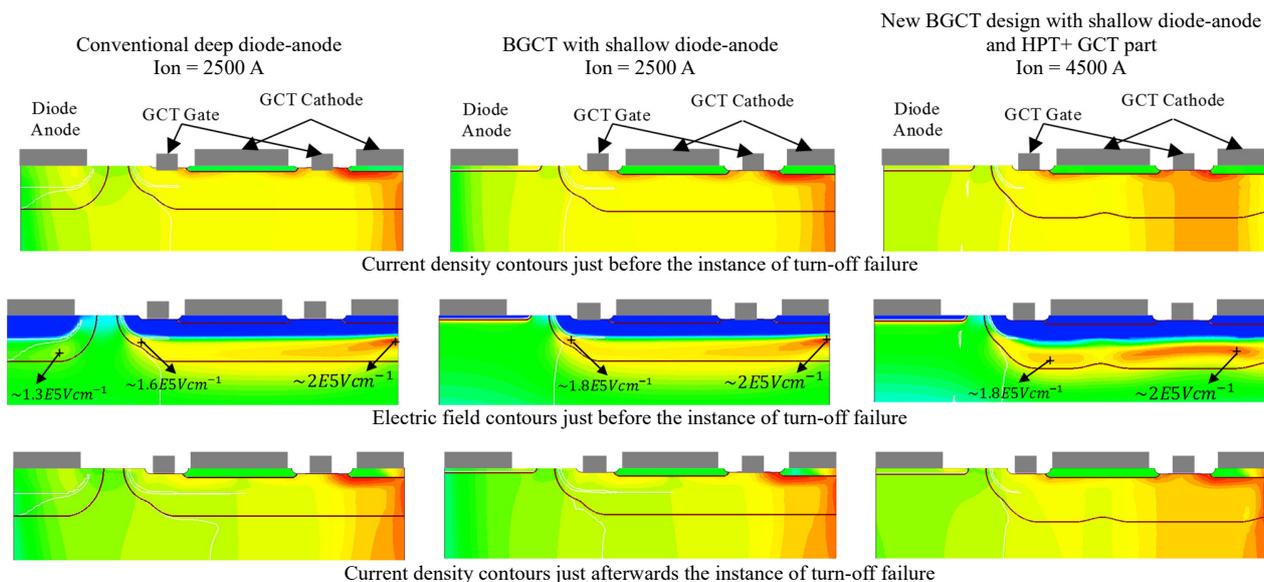


Figure 6: Current density and electric field contours just before the moment of turn-off failure depicted at Error! Reference source not found. (a, b) and just

presence of high electric field with high conduction current induces carrier generation by dynamic avalanche which leads to the catastrophic failure of the device. The location of strongest dynamic avalanche phenomenon is engineered via the HPT+ junction to be located nearer the gate electrode allows the device to turn-off successfully a much higher current level.

## VI. EXPERIMENTAL DEMONSTRATION

BGCT devices with shallow diode anodes and HPT+ GCT p-base junctions were fabricated for the first time to demonstrate the BGCT concept in large area 91mm wafers. A maximum current capability of 4.4kA at 2.8kV and 115°C was achieved, a result which is more than 1.3 times higher than the RC-IGCT. The last successful turn-off (last pass) measurement is shown in Figure 7. This verifies that BGCTs with shallow diodes and High Power Technology in the GCT part meet the requirements of high power applications.

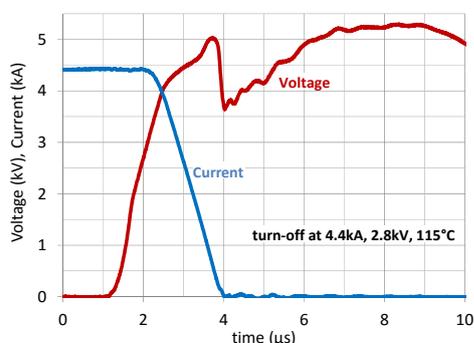


Figure 7: The measured SOA turn-off waveforms of a 91mm, 4.5kV BGCT.

## VII. CONCLUSIONS

In this paper the effect of shallow diode anodes and HPT+ GCT p-base junctions on the operation of the BGCT was analysed in detail, with focus on the current controllability of the GCT part. The simulation results suggest that BGCTs with shallow diodes do not suffer in terms of current controllability. Further, the introduction of HPT+ in the GCT part results in the increase of the MCC by up to 47% at room temperature and 58% at 400K. The fabricated 91mm BGCT with shallow diode anode and HPT+ achieved 4.4kA of MCC at 2.8kV, 115°C, more than 1.3 times higher than the maximum turn-off current capability of the RC-IGCT. This result demonstrates that BGCTs featuring shallow diode-anodes and High Power Technology maintain the performance improvements when operating in diode mode while they do get the step improvement in current controllability to become the new standard design.

## REFERENCES

[1] H. Grüning, B. Ødegård, J. Rees, A. Weber, E. Carroll, S. Eicher, and B. Odegård, "High-power hard-driven GTO module for 4.5 kV/3 kA snubberless operation," in *Power Conversion and Intelligent Motion (PCIM Europe)*, 1996, no. May, pp. 169–184.

[2] S. Klaka, M. Frecker, and H. Gruning, "The integrated gate-commutated thyristor: a new high-efficiency, high-power switch for

series or snubberless operation," in *Power Conversion and Intelligent Motion (PCIM Europe)*, 1997, pp. 597–597.

[3] U. Vemulapati, M. Bellini, M. Arnold, M. Rahimo, and T. Stiasny, "The concept of Bi-mode Gate Commutated Thyristor-A new type of reverse conducting IGCT," in *IEEE International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, 2012, pp. 29–32.

[4] U. Vemulapati, M. Arnold, M. Rahimo, J. Vobecky, T. Stiasny, N. Lophitis, and F. Udrea, "An Experimental Demonstration of a 4.5 kV Bi-mode Gate Commutated Thyristor (BGCT)," in *IEEE International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, 2015, pp. 109 – 112.

[5] N. Lophitis, M. Antoniou, F. Udrea, U. Vemulapati, M. Arnold, I. Nistor, J. Vobecky, and M. Rahimo, "Improving Current Controllability in Bi-mode Gate Commutated Thyristors," *IEEE Trans. Electron Devices*, vol. 62, no. 7, pp. 2263–2269, Jul. 2015.

[6] N. Lophitis, M. Antoniou, F. Udrea, U. Vemulapati, M. Arnold, I. Nistor, J. Vobecky, and M. Rahimo, "New Bi-mode GCT design concept for high current controllability and low on state voltage drop," *IEEE Electron Device Lett.*, 2016.

[7] T. Wikstrom, T. Stiasny, M. Rahimo, D. Cottet, P. Streit, and T. Wikström, "The Corrugated P-Base IGCT - a New Benchmark for Large Area SOA Scaling," in *IEEE International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, 2007.

[8] M. Arnold, T. Wikstroem, Y. Otani, T. Stiasny, and M. Rahimo, "High Temperature Operation of HPT + IGCTs," in *PCIM Europe*, 2011.

[9] K. Satoh, K. Morishita, N. Hirano, M. Yamamoto, and A. Kawakami, "New design approach for ultra high power GCT thyristor," in *IEEE International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, 1999.

[10] K. Satoh, T. Nakagawa, M. Yamamoto, K. Morishita, and A. Kawakami, "6 kV/4 kA gate commutated turn-off thyristor with operation DC voltage of 3.6 kV," in *IEEE International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, 1998, pp. 205–208.

[11] M. Bakowski and U. Gustafsson, "The two basic failure modes in the GTO - modelling and experiment," in *IEEE International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, 1995, pp. 354–368.

[12] N. Lophitis, M. Antoniou, F. Udrea, I. Nistor, M. Arnold, T. Wikström, and J. Vobecky, "Parameters influencing the maximum controllable current in gate commutated thyristors," *IET Circuits, Devices Syst.*, vol. 8, no. 3, pp. 221–226, May 2014.

[13] N. Lophitis, M. Antoniou, F. Udrea, F. D. Bauer, I. Nistor, M. Arnold, T. Wikstrom, and J. Vobecky, "The Destruction Mechanism in GCTs," *IEEE Trans. Electron Devices*, vol. 60, no. 2, pp. 819–826, Feb. 2013.

[14] N. Lophitis, M. Antoniou, F. Udrea, I. Nistor, M. T. Rahimo, M. Arnold, T. Wikstroem, and J. Vobecky, "Gate Commutated Thyristor With Voltage Independent Maximum Controllable Current," *IEEE Electron Device Lett.*, vol. 34, no. 8, pp. 1–1, Aug. 2013.