New Bi-Mode Gate-Commutated Thyristor Design Concept for High-Current Controllability and Low ON-State Voltage Drop

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New Bi-mode Gate Commutated Thyristor design concept for high current controllability and low on state voltage drop

N. Lophitis, M. Antoniou, U. Vemulapati, M. Arnold, I. Nistor, J. Vobecky, M. Rahimo, F. Udrea

Abstract—A new design approach for Bi-mode Gate Commutated Thyristors (BGCTs) is proposed for high current controllability and low on state voltage drop. Using a complex multi-cell mixed mode simulation model which can capture the Maximum Controllable Current (MCC) of large area devices, a failure analysis was performed to demonstrate that the new design concept can increase the MCC by about 27% at room temperature and by about 17% at 400K while minimising the on-state voltage drop. The simulations depict that the improvement comes from the new approach to terminate the Gate Commutated Thyristor (GCT) part in the BGCT way of intertwining GCT and diode regions for reverse conducting operation.

Index Terms— Full Wafer Modelling, Bi-mode, Gate Commutated Thyristor, BGCT, GCT, Maximum Controllable Current, MCC, Safe Operating Area, SOA, Thyristor, Reverse Conducting.

I. INTRODUCTION

Electronic devices with high power rating are increasingly being used in power transmission and distribution. Thyristor devices such as the Integrated Gate Commutated Thyristor (IGCT) [1] offer certain advantages that make them particularly attractive for these applications. In voltage source inverter applications, the monolithic integration of diodes with the semiconductor switch brings down the component count and reduces the system design complexity. As a result the system reliability improves [2], [3]. The Bi-mode Gate Commutated Thyristor (BGCT) is a new reverse conducting device concept which has improved operation characteristics over the conventional Reverse Conducting Gate Commutated Thyristor (RC-GCT) [4]. The first experimental demonstration of this concept was presented in [5] whereas the requirements for high current controllability in Bi-mode GCTs were analysed in [6]. In this paper a new design is proposed which supersedes the conventional design optimization methodology for high Maximum Controllable Current (MCC), further improves the MCC and minimises the on-state losses. It therefore provides an improved design concept for the GCT part in the Bi-mode GCT arrangement which solves the pressing demand of lowering the ON-state losses and increasing the MCC for the next generation GCT-like devices. A multi-cell mixed mode simulation model for large area devices is used in
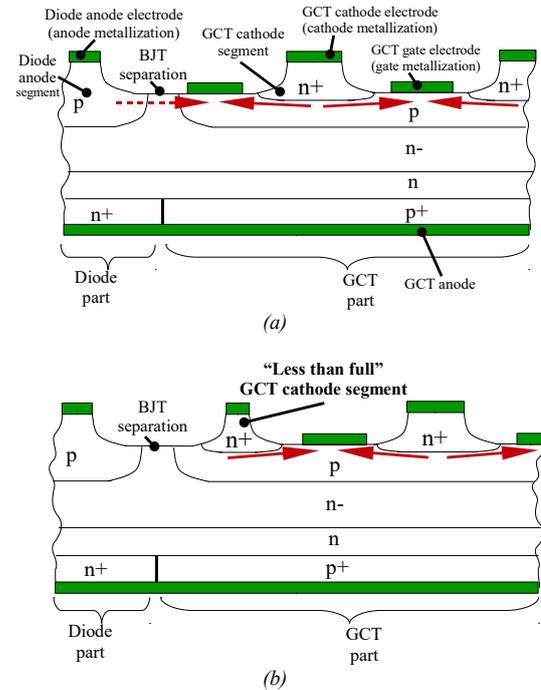

Figure 1: BGCT (half-cell) schematic illustration. The red arrows present the current flow path during turn-off. (a) Conventional design optimised for high MCC: the GCT p-base in the proximity of the separation includes a gate contact. (b) New BGCT: The GCT part comprises a "less than full" (e.g. half) GCT cathode segment to terminate the GCT part.

this work to assess and compare the new design with the conventional.

II. NEW BGCT CELL DESIGN

When compared to the conventionally optimised BGCT design [6] shown in Figure 1a, the new design depicted in Figure 1b, features the same diode and p-n-p Bipolar Junction Transistor (BJT) separation region, equal cell dimensions, cathode, anode and gate region area. The novelty lies in the cathode segment arrangement and cathode area distribution of the GCT part: in the new BGCT, the three full sized identical GCT cathode segments that are normally found in a 3:1 GCT:Diode BGCT are split in two full sized segments and two "*less than full*" (e.g. half sized) segments. The "less than full" cathode segments are placed in the proximity of the diode separation to terminate the GCT part of the BGCT whereas the full sized segments are placed in the middle of the GCT part.

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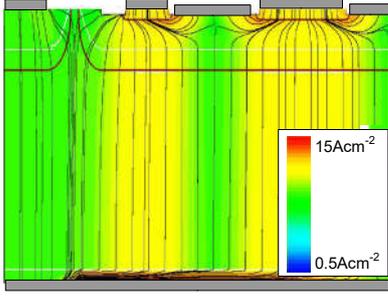
Figure 2: Current density contours and current flow lines at room temperature during the initial phase of the GCT turn-on procedure
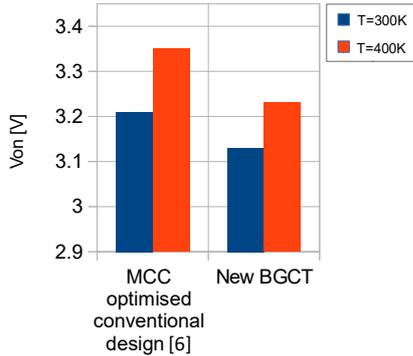

Figure 3: GCT on-state voltage drop of the new BGCT compared to the MCC optimised conventional design. $I_{ON} = 3500A$, T = 300K and T = 400K.

Further, the GCT p-base region in the proximity of the diode is reduced and no GCT gate metallisation is included in the GCT p-base region next to the diode part.

III. METHODOLOGY FOR DEVICE SIMULATIONS

In order to assess full wafer devices in terms of the Maximum Controllable Current a number of two dimensional and three dimensional models have been proposed [6]–[9]. In this paper, the model developed for BGCTs in [6] is used which allows us to directly compare the new design with its state-of-the-art conventional counterpart. It accounts for current redistribution in the wafer device during turn-off due to parasitic uneven gate inductive loading and it can successfully capture the turn-off failure in TCAD simulations which takes part due to uneven delay in the turn-off signal in different regions of the wafer. In this model, a BGCT wafer device consists of two Finite Element Method (FEM) BGCT cells which are interconnected with wires defined using a compact model. They represent two regions that can be distinguished in a wafer device in terms of how fast they switch off, specifically the "*region that turns off last*" and the "*bulk*" of the device. The "*region that turns off last*" experiences an increased gate inductance and therefore a
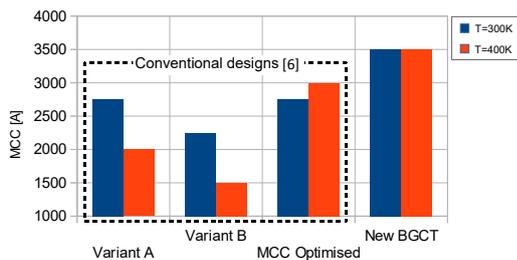

Figure 4. MCC capability of the new BGCT design featuring half segment as the terminating "less than full" segment in comparison to other conventional design variants at T = 300 K and T = 400 K, $V_{dc} = 2.7$ kV.

delayed turn-off signal. Both FEM cells feature an identical doping profile but are scaled up to make up for the approximate area of the equivalent wafer region that they represent. A total active area of $40cm^2$ is assumed for the 4.5 kV voltage class.

An MCC test requires the facilitation of many turn-off simulations before a turn-off failure is recorded. The procedure followed and the conditions for considering a turn-off to be successful are described in [6]. The current level at the last successful (last pass) turn-off defines the Maximum Current Controllability.

IV. TURN-ON AND ON-STATE

Large area thyristor devices are prone to hot-spot formation and premature failure if the turn-on is uneven. This is more likely to occur when turning on at low temperature and it can be avoided with proper design of the GCT gate/cathode interdigitation. The current density contours at the first instance of the turn-on for the new BGCT design featuring half segment as the terminating "less than full" segment is depicted in Figure 2. As shown, the gate current is injected in the GCT p-base uniformly and all cathode segments start injecting homogeneously. Figure 3 depicts how the on-state voltage drop of the new BGCT compares to the drop of the conventional design optimised for MCC in [6]. The lower voltage drop is the result of the GCT cathode segments being spread over a wider area in the new design which in turn improves plasma distribution and silicon utilisation once the GCT part is fully on.

V. CURRENT CONTROLLABILITY

The results of the MCC test of the new design featuring half segment as the terminating "*less than full*" segment are compared with those of typical variants of classic BGCT designs in Figure 4. The latter were originally published in [6] and are included here with the aim of enhancing the clarity. As shown, the new design achieves higher current controllability
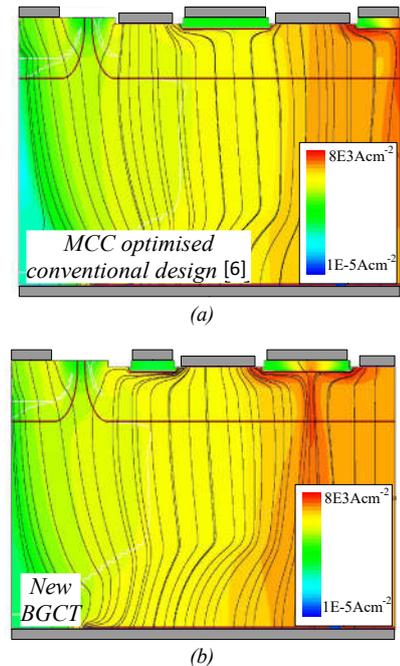

(a)

(b)

Figure 5. Turn-off current density with current stream traces at the onset of turn-off failure at T = 300 K, V_{dc}=2.7kV. (a) Conventional design optimised for high MCC ("region to turn off last" I_{on}= 3000 A). (b) New BGCT design featuring half segment as the terminating "less than full" segment ("region to turn off last", I_{on} = 3750 A).
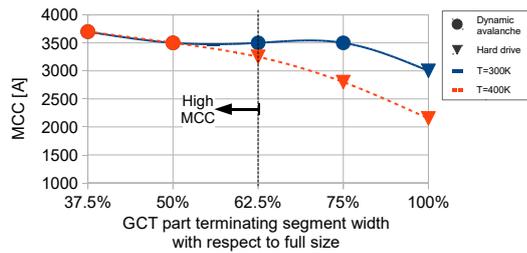
Figure 6. MCC capability of the new BGCT design with respect to the segment size in the proximity of the diode at T=300K (–) and 400 K (--), $V_{dc} = 2.7$ kV. The failure mechanisms, failure due to dynamic avalanche retriggering (●) and due to violation of the hard drive (▼), are also marked.

in the MCC simulation test both at room temperature and at high temperature. The improvement when compared to the conventional BGCT optimised for high MCC is about 27% at room temperature and about 17% at high temperature. Figure 5 depicts the current density with current stream traces of the "*region that turns off last*" at the instance of failure for the new design (Figure 5b) and its conventional counterpart optimised for high MCC (Figure 5a). The new BGCT operates at the realm of hard drive and fails at a later stage in the turn-off due to dynamic avalanche induced thyristor re-triggering, a failure phenomenon that is identical with the failure mechanism of the conventionally optimised BGCT for high MCC [6] and other asymmetric GCTs at standard operation conditions [9]. The positioning of cathodes in the new arrangement (over a wider area) lowers the peak current density in the active area during conduction and therefore the carriers' generation by dynamic avalanche at fixed current level. Further, the longest lateral distance in the holes path during turn-off is made equal for all cathode segments which ensures the uniformity of the extraction of carriers during turn-off. As a result, BGCTs following the new design concept compared to the conventional method for optimizing a BGCT for high MCC can sustain higher current and can have an increased maximum controllable current.

When the temperature is increased there exists a proportional decrease in the cathode/p-base junction voltage. Hence, a reduced conduction current is required for the built-in junction voltage to be overcome. At the same time, the avalanche coefficients are reduced, the adverse effects of dynamic avalanche become weaker and an increased conduction current is required for the built-in junction voltage to be overcome. Therefore the trend of the MCC with temperature can be positive, i.e. higher MCC with increasing temperature or negative, i.e. lower MCC with increasing temperature. The device design can indeed affect which one of the two dominates and therefore the trend. As already mentioned, the new design fails due to a dynamic avalanche induced re-triggering, a failure mechanism where the MCC is affected both by the avalanche coefficients and the junction voltage also. It achieves the same MCC value at both 400K and room temperature because the effect of the change in the avalanche coefficients is balanced by the effects of the change in the junction voltage.

Simulations were also set-up to investigate how the width of this cathode segment affects the MCC and the failure mechanism. Figure 6 summarises the MCC capability of the new BGCT for different "*less than full*" segment widths. The failure mechanism for every BGCT investigated was also checked. A failure due to dynamic avalanche re-triggering is

marked with a full circle whilst a failure due to hard drive with a full triangle. The MCC results at room temperature are marked with a solid line and at 400K with a dotted line. As shown, at room temperature the dominating failure mechanism is dynamic avalanche induced retriggering. Also the MCC is practically unchanged for a wide range of segment widths measuring a maximum 75% of the full segment size. When the GCT part is terminated with a full sized (100%) cathode segment, the failure mechanism changed to failure due to the violation of the hard drive criterion which in turn gave a drop in the MCC. At 400K the devices with terminating segment width of less than 62.5% of full size failed due to avalanche induced retriggering and the MCC was found to stay unaltered. Those with terminating cathode segment of 62.5% and more had a considerable MCC drop due to the failure being induced by the violation of the hard drive criterion. Under this failure mechanism, the MCC reduces with the increase of the temperature due to the reduction of the junction voltage and its adverse effect on the hard drive limit. Considering these results, the optimum design for the new BGCT features cathode segments in the proximity of the diode with width smaller than 62.5% of the full cathode segment width. This upper limit should not be exceeded due to the switch in the failure mechanism at high temperature and the resulting rapid decline of the MCC once this limit is passed.

VI.   CONCLUSIONS

A new design concept for Bi-mode GCTs is introduced which can significantly augment the current controllability and simultaneously lower the conduction losses. The new arrangement of the cathode area and the interdigitation of the gate electrodes in the GCT part ensures a safe and uniform turn-on and turn-off operation, improved plasma distribution and extraction and lower dynamic avalanche carriers' generation. Compared to a conventional design optimised for high MCC, the proposed new design concept further improves the MCC by 27% at room temperature and by 17% at high temperature. At the same time the conduction voltage drop is also marginally lowered. It therefore offers an optimum method for gate/cathode interdigitation when designing the GCT part of Bi-mode GCTs.

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