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Generic SPWM Technique for Multilevel Inverter

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Abstract - Multilevel inverters generate stepped AC signals and thus overcome many of the limitations with the classical inverter circuit. Multilevel inverters use many number of switches and generate staircase type output through controlled switching of various switches. The sequence of switching and the duration of each step are very vital in minimizing the THD. The methods of generating gating signals are not unique. Many methods that are proposed in literatures make use of SPWM technique. Sinusoidal Pulse Width Modulation (SPWM) is a popular control method widely used in power electronic inverter circuit. It has advantages like low switching losses, the output has fewer harmonic and method is easy to implement. The different SPWM methods are: (A) Phase Disposition PWM (PDPWM), (B) Phase Opposition Disposition PWM (PODPWM), (C) Alternative Opposition and Disposition PWM (APODPWM), (D) Phase Shift PWM (PSPWM), (E) Carrier Overlapping PWM (COPWM) and (F) Multi Carrier Sinusoidal Pulse Width Modulation with Variable Frequency (MCSPWMVF). All the above methods make use of many triangular signals, that are level shifted or phase shifted, and compare with a single sine wave to generate gating signals for the respective switches. The intersection of the sine signal with the various triangular signals will generate the gating signals for the respective switches. In the present investigation a generalized gating signal generation method is proposed using only one modulating and one carrier signal. The signal so generated is steered into various switches through pulse steering circuit developed in the present work.

Keywords—Educational tools, Inverter operation, Battery Energy Storage System, Energy Storage System, active filter.

I. Introduction

In recent times, inverters have found its way into many fields of power system research works, particularly in the area of the applications of power electronics for power system applications, such as FACTS, Energy Storage Systems and active filters. Multilevel inverters are class of inverters in which stepped AC signals are generated using many switches so as to minimize dv/dt and THD. As the structure of the multilevel inverter varies from topology to topology and also from the traditional inverter, the closed loop system requires different SPWM techniques discussed below [1].

The main objectives of the present paper are to review some of the SPWM methods used in multilevel inverter and to propose a generic method which makes use of one sine and one triangular signal.

The introduction to various methods is given in II, the proposed SPWM technique is presented in III, simulation results from the proposed method are presented in IV followed by conclusion in V.

II. Various Types of SPWM Techniques

A. Phase Disposition PWM (PD) [2]

In this method all the carrier signals of same frequency, amplitude and phase, but having different DC offset to occupy different levels, are compared with a single sine modulating signal. The intersection points of the modulating signal with the respective triangular signals are the points, where the gating signals for the switches of respective levels are generated. Since all carrier waves are selected with the same phase, the method is called as PD. The method is illustrated in the Fig.1. in which the number of triangular signals required is (n-1) where n = number of levels.

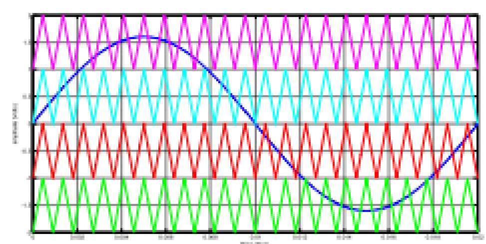

Fig. 1. Phase Disposition PWM

B. Phase Opposition Disposition PWM (POD) [3]

This method also contains carrier signals with same frequency, amplitude but differ in phase, the carrier signals above reference zero voltage are in 180^o out of phase with the carrier signals bellow the zero reference voltage, this method is illustrated in the Fig. 2. [3]

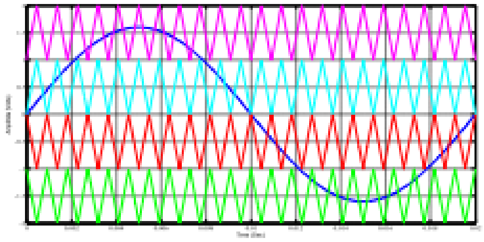

Fig. 2. Phase Opposition Disposition PWM

C. *Alternative Phase Opposition Disposition PWM [2]*

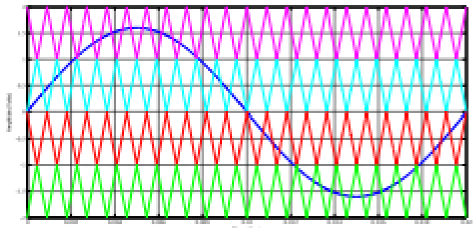

Fig. 3. APOD PWM

This method also contains carrier signals with same frequency and amplitude but each carrier wave is 180^{o} out of phase with the adjacent one, this method is illustrated in the Fig. 3. [2]

D. *Phase Shift PWM [3]*

In this method all carrier signals have same amplitude, frequency and DC offset but they are phase shifted to each other by 90^{o}, this method is illustrated in the Fig. 4. [3]

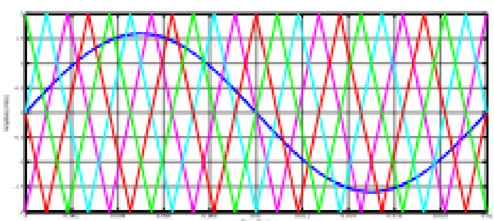

Fig. 4. Phase Shift PWM

E. *Carrier Overlapping PWM [4-5]*

In this method for an m-level inverter, m-1 carrier signals are used which have the same frequency and same peak to peak amplitude. The carrier signals are disposed such that the band they occupy overlap each other and overlap each other till half of its amplitude, and the reference signal is centred in the middle of the carrier signals, this method is illustrated in Fig. 5.

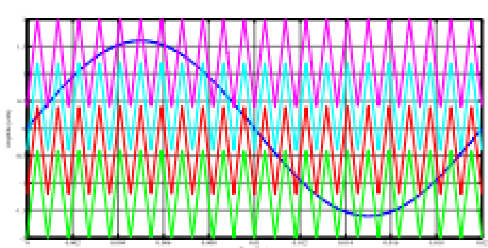

Fig. 5. Carrier Overlapping PWM

F. *Multi Carrier Sinusoidal Pulse Width Modulation with Variable Frequency PWM [4-5]*

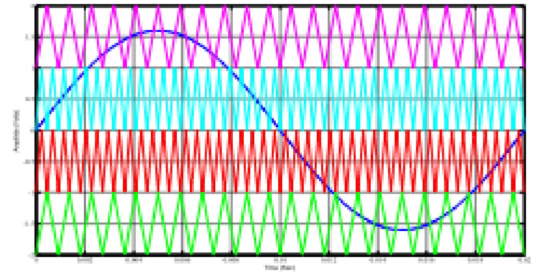

Fig. 6. Multi Carrier Sinusoidal Pulse Width Modulation with Variable Frequency PWM

This method is used for multilevel inverters where the switching frequency of the upper and lower switches is more than the intermediate switches, this method is used to equalize the member of switching's, this method is illustrated in Fig. 6.

III. PROPOSED SPWM TECHNIQUE

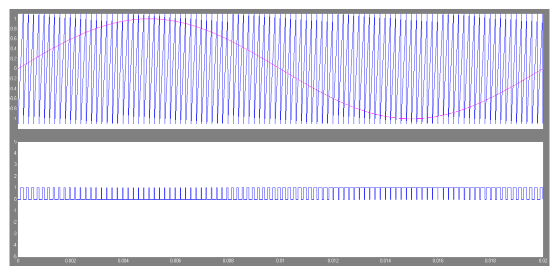

Fig. 7. Parent Signal

In the Novel SPWM technique proposed, first a parent signal is obtained by comparing a reference sine wave with a triangular carrier wave as shown in fig. 7., and then the pulse trains are steered into the respective switches at appropriate time intervals using logic combinations as depicted in fig. 8. – fig. 10. Fig. 8. shows the scheme of generation of the parent SPWM signal, fig. 9. and fig. 10. shows the pulse steering logic scheme to apply gating signals to a particular switch. Thus generating gating signals for any switch involves logical ANDing of the parent signal with a pulse of duration equal to the conduction period of that switch.

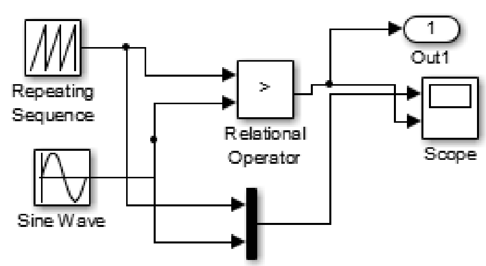

Fig. 8. MATLAB-SIMULINK model of Parent signal generation

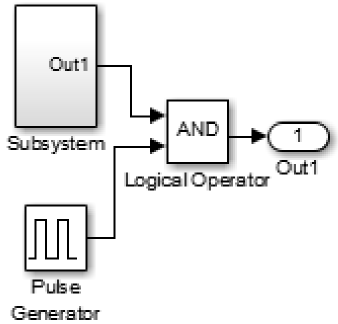

Fig. 9. MATLAB-SIMULINK model for signal generation

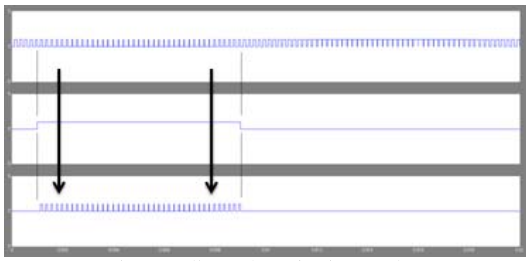

Fig. 10. Illustration of pulse steering

The presented method makes use of only one sine and one carrier signal and is generic in nature. As a result the method can be extended to any types of multilevel inverter by generating a parent train of pulses and then steering them to appropriate switches to generate required step signal.

IV. SIMULATION RESULTS OF THE GENERIC METHOD

Simulation studies have been carried out on basic three different types of multilevel inverters; diode clamped, capacitor clamped and cascaded H-bridge type shown in figures 11-13, using the proposed SPWM method. Figures 14-19 show the output voltage and the harmonics data of the voltage from the respective MLI circuits. The switching states of diode clamped and capacitor clamped remains same but for cascaded H-bridge type following switching sequence is followed as per Table I. In order to compare the proposed PWM method with other methods given in [2] & [3], the cascaded H-bridge type is simulated using five different methods and harmonic data using Nyquist frequency tabulated in Table II.

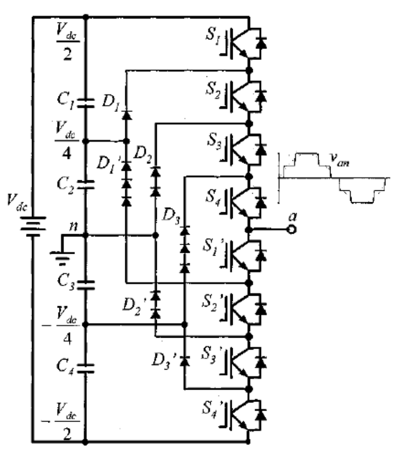

Fig. 11. Diode Clamped Multilevel Inverter (DCMLI)

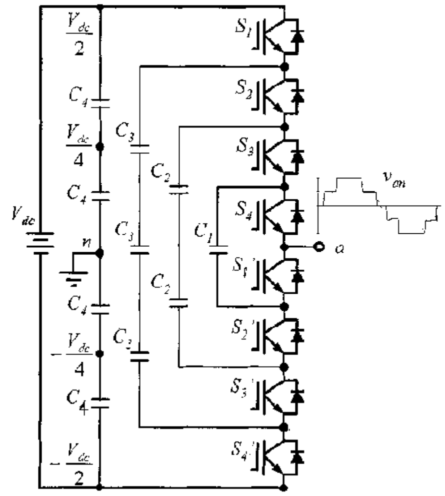

Fig. 12. Capacitor clamped multilevel inverter (CCMLI)

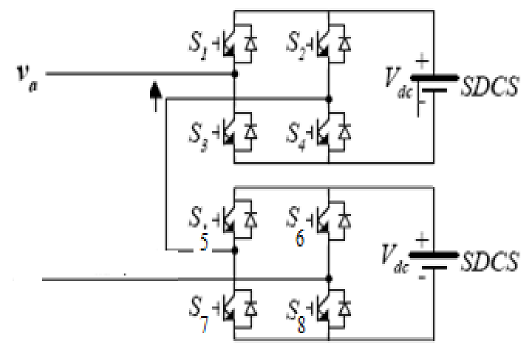

Fig. 13. Cascaded H-bridge Multilevel Inverter (CHBMLI)

V/ S	S1	S2	S3	S4	S5	S6	S7	S8
0	0	0	1	1	0	0	1	1
V	1	0	0	1	0	0	1	1
2V	1	0	0	1	1	0	0	1
-V	0	0	1	1	0	1	1	0
-2V	0	1	1	0	0	1	1	0

Table I: Switching states of CHB MLI

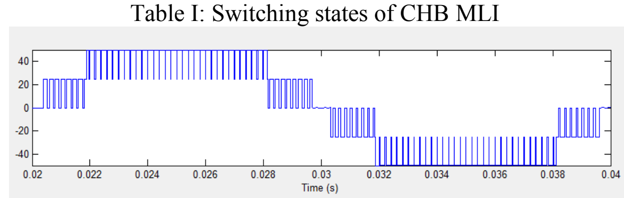

Fig. 14. Output Voltage of DCMLI

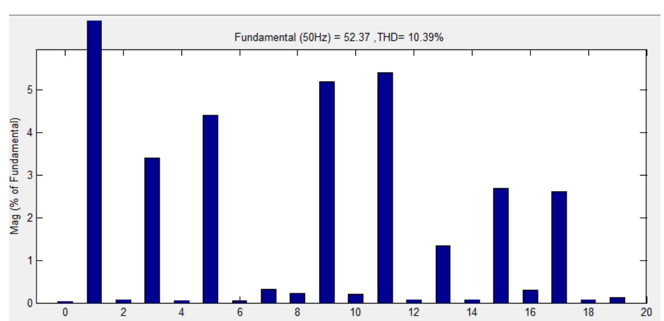

Fig. 15. Harmonics data from DCMLI

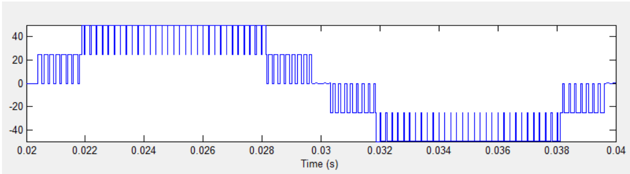

Fig. 16. Output Voltage of CCMLI

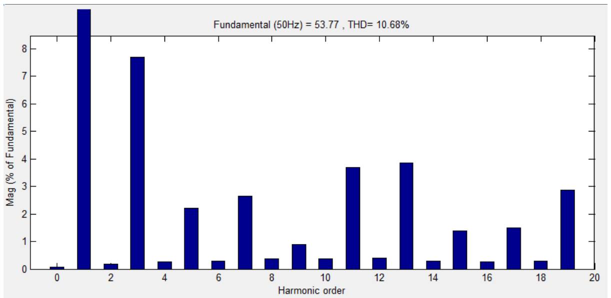

Fig. 17. Harmonics data from CCMLI

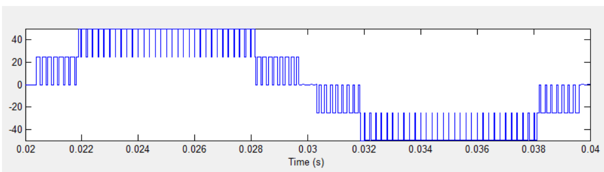

Fig. 18. Output of CHBMLI

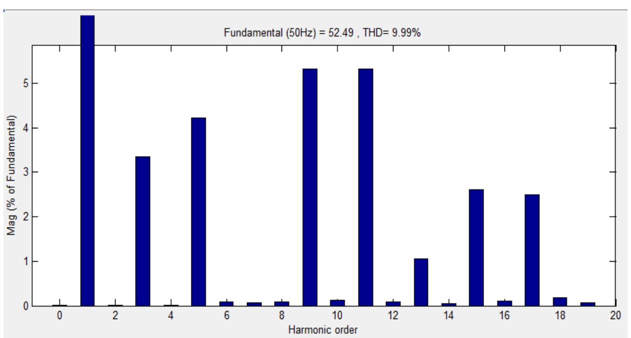

Fig. 19. Harmonics data from CHBMLI

Method	THD
PD	32%
POD	32.01%
APOD	32.04%
VF	32.5%*
CO	36.4%*
New Method	26.69%

* contains DC component(wave is not symmetrical)

Table II
THD OF CASCADED H-BRIDGE MLI FROM DIFFERENT METHODS

V.RESULTS

The advantages of the method is that it is generic and pulses can be generated for topologies that require unsymmetrical gating signals

VI. CONCLUSIONS

Several control techniques for various multilevel inverters are discussed and compared with the new generic type of PWM control. The new method is very generic in nature and can be applied to any type of MLI irrespective of the level. The main advantage of the proposed control is that only one sine and carrier wave is employed unlike other control methods proposed in the literature, where n-1 number of carrier waves are required. Also the control results in lower THD compared to other methods. Further work is in progress to improve the proposed technique with a view to minimizing the THD.

FUTURE WORK

Future work is underway to test the concept on three phase topologies which will be reserved for future correspondence

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3) K. Narayana Swami received the B.E. degree in Electrical Power from Mysore, India in 1986 and received the M.E. degree in Power Systems from Bangalore, India in 1994 and perusing Ph.D degree in Power Electronics from Kuvempu University, India. He worked as Lecture and Senior lecture in the Electronics and Communication Engineering department of S.J.C. Institute of Technology, Chickballapur, India from 1987-2001. He later joined Sri Venkateshwara College of Engineering, Bangalore, India as Assistant Professor from 2001-2008. Then he joined REVA ITM, Bangalore, India as professor in 2009 and presently working as Senior Associate Professor. He is pursuing his Ph.D in the area of multilevel inverter