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# PLL-based Enhanced Control of Boost PFC Converter for Smart Farming Lighting Application

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ABSTRACT

Controlled environment farming has become an attractive solution to increase the food production with limited use of resources. LED lights are often used in this type of farming to increase plant yield. LED lights are dc load, whereas the grid provides ac power. This necessitates the use of power factor correction (PFC) converter as an interface between the grid and the lights. This paper proposes an innovative control method for the boost PFC converter, where an advanced phase-locked loop scheme is developed that can eliminate measurement dc offset and provide harmonic robust estimation of the grid voltage fundamental component. The applied nonlinear control uses the existing two-loop control architecture. Based on a baseline PI controller, a nonlinear function is added to make the controller react faster when it is far from the reference and vice-versa. Comprehensive simulation studies are conducted to assess the performance of the proposed method under various challenging test scenarios. Compared to the baseline method, the proposed technique achieved 42% ~ 65% reduction in total harmonic distortion depending on the test cases, which makes the technique a suitable candidate for improving the operational efficiency and, consequently, the running cost of a smart farming lighting system on an industrial scale. Results show the effectiveness of the proposed method over the conventional counterpart.

## Introduction

Anthropogenic climate change is a serious concern of our time and ever-increasing carbon emissions are playing a major role in this regard. This motivated the international community to come forward with the ambitious net zero emission target by 2050. Out of the various sectors, food production is responsible for roughly one-quarter of the total greenhouse gas (GHG) emissions [1]. So, decarbonising this sector will be essential if we are to achieve the net zero emission target in time. However, this is going to be very challenging as the food production will have to increase by 70% to meet the ever-growing population by 2050 [2]. As the cultivable land area is declining, further intensification of farming needs to take place by using additional natural resources to meet the increasing food demand, which could potentially cause further increase in GHG emission. This necessitates the development of advanced farming techniques that can increase food production in a sustainable manner without requiring additional cultivable lands and/or natural resources.

Speed breeding [3] has appeared as a emerging solution to the aforementioned problems. In speed breeding, plant growth can be accelerated by manipulating the environmental conditions in smart greenhouse settings, thereby increasing the number of farming cycles per year and production output without increasing the cultivable land area. Often this is accomplished by using artificial lights that mimic the natural day-night cycle but in a controlled environment agriculture (CEA). An early work in this area [4] showed that by artificially controlling the photo-period, i.e., length of the day, it is possible to double the crop production compared to the conventional counterpart. An overview of the CEA setup is given in Fig.1. This figure shows that light emitting diode (LED) drivers are used in a CEA setup to manipulate the LED lights, which ultimately regulate the photo-period of the plant. As photo-period is one of the key control variables in the CEA, LED drivers play an important role in ensuring high-performance operation of the overall system. An efficient LED driver will lower the operation costs and

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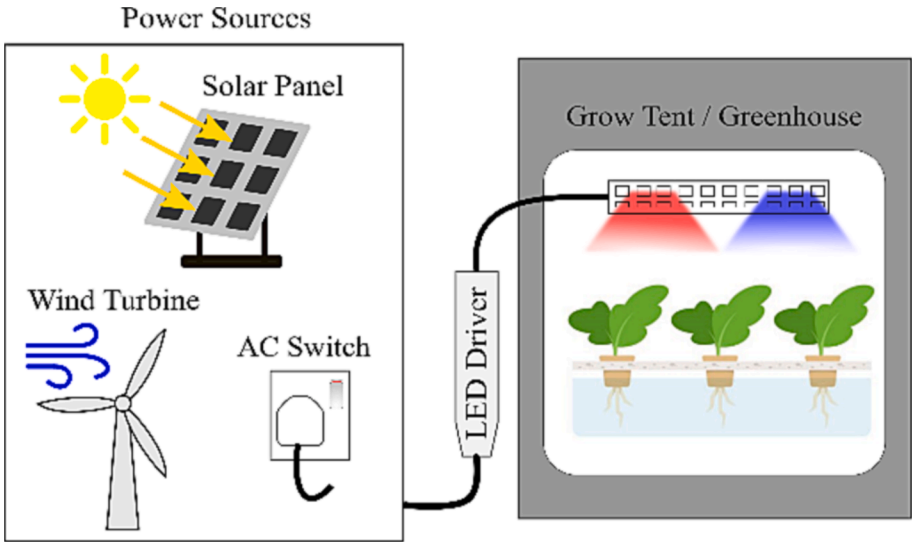


**Figure 1.** An overview of the LED controlled smart farming.

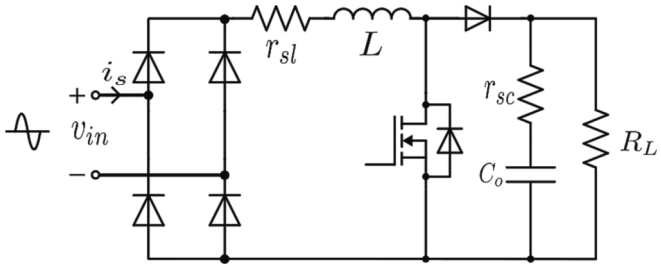


**Figure 2.** Circuit diagram of a boost PFC converter.

reduce the GHG emission of the overall system [5,6,7]. In addition, if the LEDs are powered by renewable energy sources, then, this will make the whole operation sustainable from an energy point of view. This motivated us to focus on the improvement related to the LED driver in this work.

LEDs require dc voltage and currents, while the grid provides ac voltage and currents. LED drivers act as an interface between the ac and dc systems.

An LED driver is typically an ac/dc converter, which provides dc output while at the same time ensure high power-factor to meet the regulatory requirement set by various standards, e.g. IEEE Std 519-2014 [8]. Power converters are widely used across various engineering applications to ensure high-performance operation of the considered systems [9,10,11,12]. In the LED driver case, numerous ac/dc converters with power factor correction (PFC) capabilities are reported in the literature. These converters typically operate in two-stages. In the first-stage, the ac power is converted into pulsating dc through a rectifier, which is often a diode-bridge-type. In the second stage, a dc-dc converter is employed for the dc voltage regulation. Most PFC converters use a step-down transformer to provide galvanic isolation and also to reduce the voltage level, which enables a low voltage level circuit implementation. Some of the popular PFC-type LED driver topologies are boost converter [13], interleaved-boost converter [14], flyback converter [15], Cuk converter [16], Sheppard-Taylor converter [17], totem-pole converter [18], etc., to name a few. For a detailed review on this topic, interested readers may consult [5,19] and the references therein. Out of the various available converters, boost PFC converter was selected in this work due to its simple structure and wide popularity for reliable long-term operation.

In this work, control of a boost PFC converter has been considered to improve the performance and efficiency of the smart farming system. Owing to its popularity, numerous control methods have been proposed in the literature for boost PFC converters. Conventionally, a two-loop architecture is the most popular one in the research and industrial literature [20]. In this method, a voltage controller works as the outer-loop, which is also the slower one while a fast current controller works as the inner-loop, which also generates the Pulse Width Modulation (PWM) signal for driving the switch(es) of the converter. In addition, a grid-voltage detection scheme is also required that extracts the real-time information of the grid and contributes to generate the reference current for the inner-loop current controller.

The existing literature on two-loop control systems for PFC converters covers a wide array of methods [19,20]. In general, proportional-integral (PI) is a popular choice for the PFC controllers. A PI controller is easy to implement, has analytical tuning rules and can be implemented without having precise information about the system parameters. However, the response is slow and there is a trade-off between the dynamic response of the converter versus the disturbance rejection capability. This motivated researchers to propose advanced controllers for the PFC converter. In [21], the authors have proposed a fuzzy logic voltage controller (FLC) for the boost PFC converter. However, no grid detection scheme is applied. This makes the controller ineffective to deal with distortion in the grid voltage. A fixed-frequency sliding mode current controller is proposed in [13]. However, as the outer-loop remained PI controlled, this may slow down the system response when the output voltage faces significant disturbances. An input-output linearisation (IOL) controller is proposed in [22]. Despite its advantages, this method is sensitive to system parameter variations. As the converter ages, system parameters may differ greatly from the nominal value, thereby significantly deteriorating the control performance. Linear active disturbance rejection voltage controller (ADRC) for boost PFC is proposed in [23]. This method improves the voltage loop controller performance compared to the conventional PI controller, however, it is still sensitive to disturbances in the current loop as that controller is still the conventional one. This limits the overall control performance. Model predictive controller with moving average is proposed in [24]. Such controller requires an accurate value of the boost inductor, which may vary significantly over the long operation of the converter. As such, it is not possible to ensure high-level control performance in wide operating conditions.

Grid-detection scheme is an integral part of the two-loop PFC controller. A fast and accurate grid-detection scheme can extract the fundamental component of the grid voltage even when the grid is

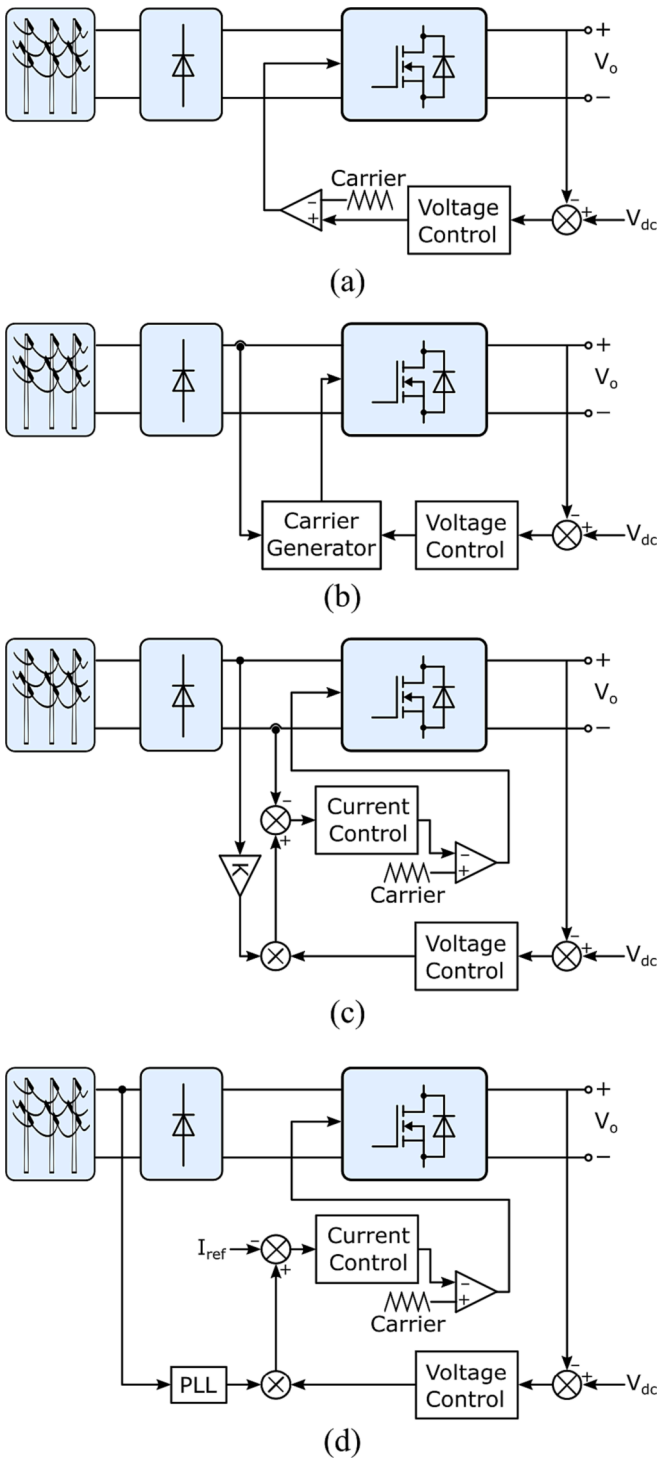


**Figure 3.** Typical control techniques used in LED drivers. (a) Type I, (b) Type II, (c) Type III, (d) Type IV.

heavily distorted. The existing grid-detection schemes for PFC converters often rely on phase-locked loop (PLL). A two-sample PLL for boost PFC has been proposed in [25]. This PLL generates a quadrature signal using finite-difference method, which is required for the PLL implementation. However, it can be sensitive to noise. A running-average filter-based PLL is proposed in [26]. This PLL utilises second-order generalised integrator (SOGI) [27] for the orthogonal signal generation while the running-average filter dc offset rejection. In addition to the loop filter tuning parameters, this PLL has an additional low-pass filter to tune, which increases the tuning complexity. A single-phase

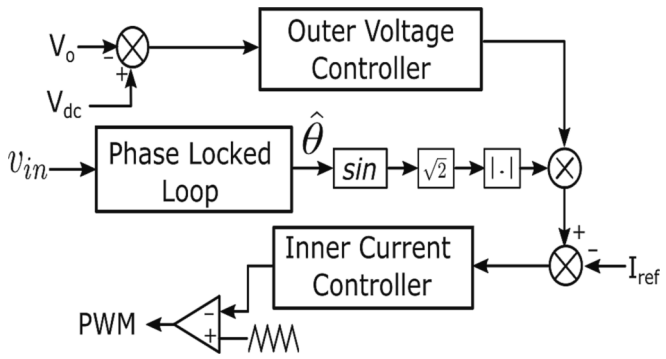


**Figure 4.** General block diagram of a Type IV control system for the boost PFC converter.

power-PLL (pPLL) with repetitive controller (RC) has been proposed for the boost PFC in [28]. However, this PLL may be susceptible to harmonic distortion due to the lack of a robust orthogonal signal generator. A digital PLL has been proposed in [29], which utilises an infinite impulse response (IIR) filter for improved harmonic robustness. However, no results are presented with distorted grid conditions. This makes it difficult to assess the performance of this PLL in the presence of grid harmonics. SOGI-PLL for boost PFC converter has been proposed in [30]. Due to its excellent band-pass filtering properties, this PLL provides good harmonic robustness. However, it is not resilient to dc offset in the measured grid voltage, thereby requiring additional filtering.

Based on the above literature review, there is a demand for an advanced control method and grid-detection scheme for effective control of boost PFC. The control scheme should be easy to implement with fast dynamic response and good disturbance rejection property. It should not be parameter dependent to ensure satisfactory control performance over a wide operating range. The grid detection scheme should be harmonically robust and insensitive to dc measurement, and the tuning should be simple. To address these issues, in this work, an enhanced nonlinear PI control scheme is applied to a boost PFC converter. Unlike the conventional method, this controller can improve the dynamic response of the system without sacrificing the disturbance rejection capability. Moreover, the core building block of this controller is the conventional PI, which makes it easy to tune and implement. For the grid-detection scheme, we propose a harmonically robust PLL scheme, which employs the quasi type-1 PLL structure and moving average filter. As a result, the proposed PLL can eliminate all odd-order harmonics in the measured grid voltage signal, which makes it suitable for meeting power quality standards, such as IEEE Std. 519- 2014 [8] and European Std. EN50160 [31]. Comprehensive simulation studies are conducted to show the feasibility of the proposed method.

The main contributions of this work are twofold. Firstly, it proposes an improved PLL scheme that can extract the phase of the fundamental grid voltage component with very low distortion. Secondly, it introduces the maiden application of the nonlinear PI control scheme for the boost PFC converter. The proposed method, comprising the PLL and the controller, results in a fast-responsive control scheme without sacrificing harmonic robustness.

The rest of this article is organised as follows: The details of the proposed PFC control method including nonlinear PI control and the grid detection scheme are given in Sec. 2. Comprehensive simulation results are given and discussed in Sec. 3. Finally, Sec. 4 concludes this article.

## Control of Boost PFC

Boost PFC converter is widely used as an LED driver. It can convert the ac grid voltage into fixed dc output voltage for driving the LED. Moreover, it also provides power factor correction, which is often

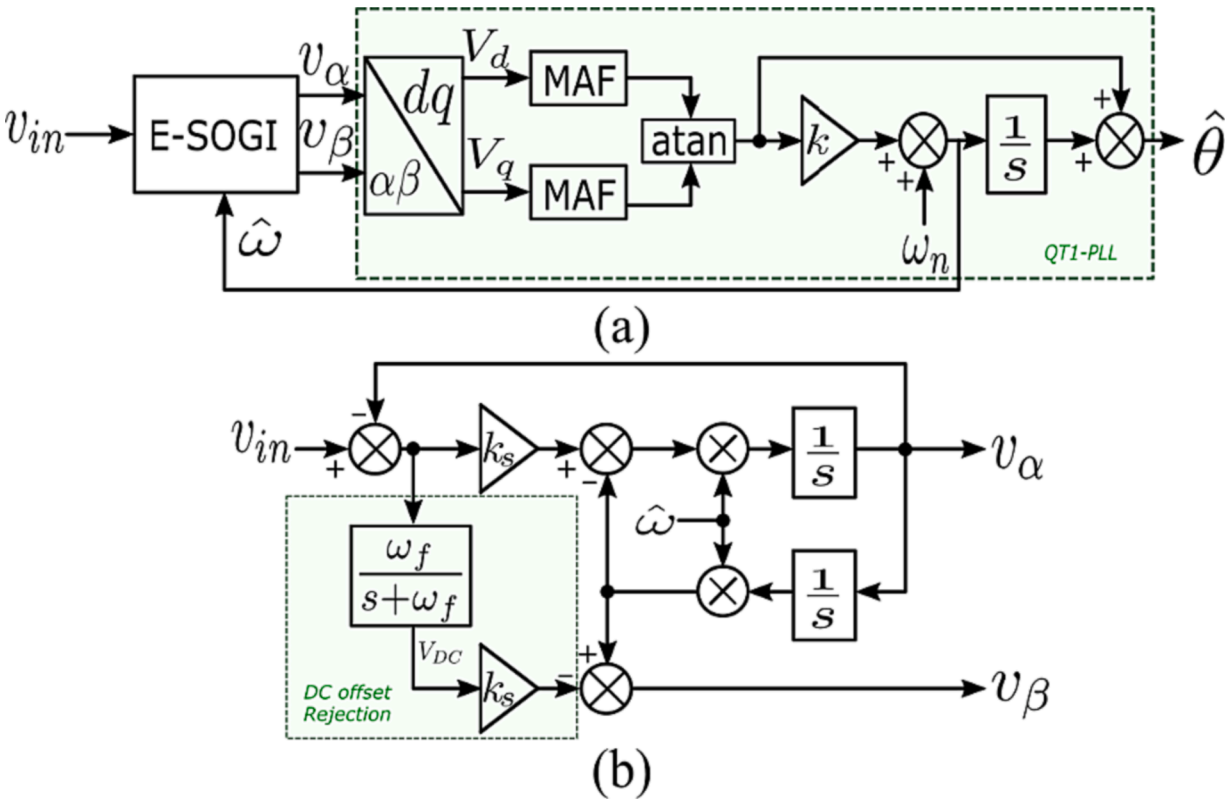


**Figure 5.** Block diagram of the proposed E-SOGI-QT1-PLL, (a) overall implementation and (b) E-SOGI implementation.

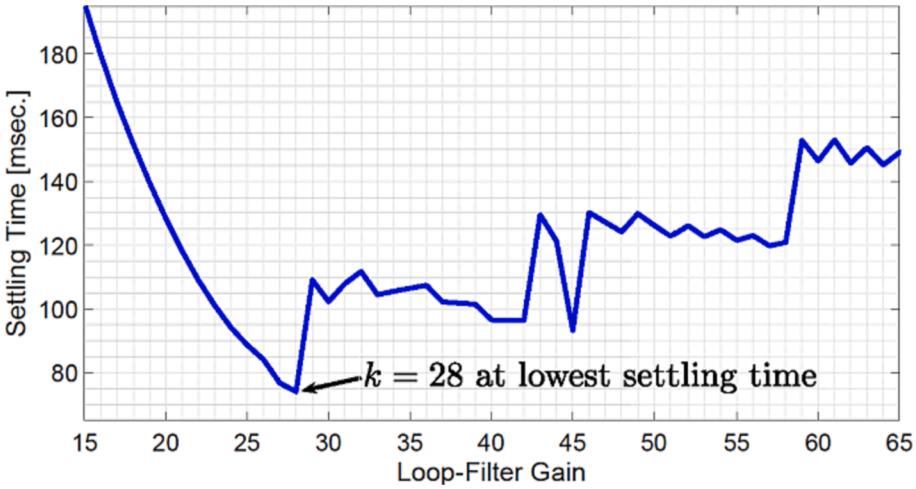


**Figure 6.** Loop-filter tuning of the proposed PLL.

mandatory for any grid-connected device over a certain power limit. The circuit diagram of a typical boost PFC converter is shown in Fig. 2 [32]. As a remark, we use upper and lower case to denote variables associated with dc and ac signals, respectively. The PFC circuit under consideration consists of two stages, namely the ac/dc and dc-dc stages. In this configuration, an H-bridge diode rectifier converts the ac input voltage $v_{in}$ into pulsating dc. This dc voltage can be approximated as $V_{dc} = V_p/\sqrt{2}$, where $V_p$ is the peak value of the ac input. It is evident that the dc voltage is lower than the peak voltage. For efficiency purposes, the reference dc-side voltage can be higher. As such, boosting up this pulsating dc voltage is taken care of by the boost converter part of the PFC circuit, which regulates the output voltage to a desired value as required by the design specification. Note that the source current, i.e., the current drawn from the ac grid is in the ac/dc stage of the PFC, therefore this current will remain ac, whereas the load current and the voltage are in the dc-dc side of the PFC, which ensures that these quantities will remain dc. Simultaneous existence of ac and dc quantities in the circuit makes it challenging to control the PFC converter. For a detailed explanation of the operation of the boost PFC converter, interested readers may refer to [32], and the references cited therein.

There are two main control requirements for the boost PFC controller. Firstly, the output voltage needs to be constantly maintained at the desired level despite changes in the grid, circuit parameters, and load. Secondly, the nonlinear current $i_s$ drawn by the PFC from the grid should have a low total harmonic distortion (THD).

To address the control objectives of boost PFC, development of the

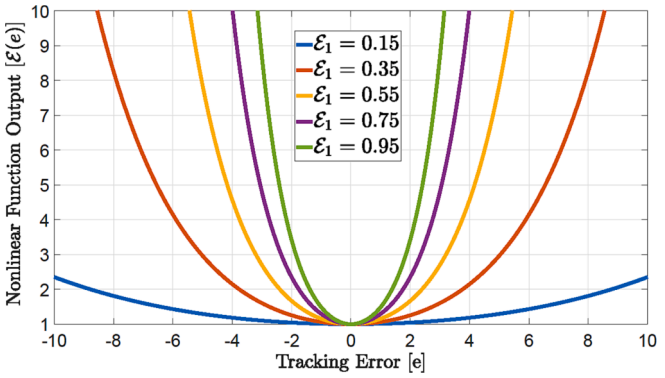


**Figure 7.** Output of the nonlinear function (8) for various $\mathscr{E}_1$ with $\mathscr{E}_0 = 1$.

control system plays a very important role. In general, control techniques used in boost PFC converters can broadly be divided into four types as shown in Fig. 3 [20]. Each type has its own merits and demerits. A type IV controller is preferable, if THD reduction is a key concern especially in the heavily distorted grid condition, whereas it comes at the cost of additional implementation complexity. Type IV control method has real time grid monitoring and self-recovery capability. It utilises the grid information in generating the PWM signal. This can maintain the performance even when there is a distortion in the grid.

A detailed block diagram of the Type IV control system of boost PFC converter is given in Fig. 4. In this method, a PLL is used to extract the fundamental component of the grid voltage, which is multiplied with the output of the outer-loop voltage controller to generate the reference current. The inner-loop current controller regulates the actual current to the outer-loop generated reference value. In general, both outer- and inner-loop controllers are of proportional-integral (PI)-type, whereas the PLL is typically the conventional synchronous reference frame PLL (SRF-PLL) [32]. In this work, two modifications are proposed. Firstly, we develop an advanced single-phase PLL that can accurately extract the fundamental component from distorted and biased grid voltage measurements. Secondly, we replace the linear PI controller by the nonlinear PI controller. These modifications are detailed in the following.

### *Grid Voltage Detection Scheme*

Single-phase grid voltage with dc offset and harmonics can be written as:

$$v_{in}(t) = V_{dc} + V_{in}\sin(\theta) + \sum_{h=3,5,\cdots} V_h \sin(\theta_h) \tag{1}$$

where the static measurement offset $V_{dc} \geq 0$, and $\theta$ are respectively the fundamental component magnitude and phase, whereas $V_h$ and $\theta_h$ are the harmonic component magnitude and phase, respectively. The objective here is to estimate $\theta$ from the measured $v_{in}(t)$. From this point, the time dependence argument of the function is omitted for notational simplicity. To estimate the $\theta$ from $v_{in}$, the single-phase quasi type-1 PLL (QT1-PLL) [33] is considered and the overview of the proposed PLL is given in Fig. 5. An advantage of the QT1-PLL

is that it uses a moving average filter (MAF). The transfer function of the MAF in continuous- and discrete-time are given by,

$$\text{MAF}(s) = \frac{1 - e^{-\mathscr{T}_c s}}{\mathscr{T}_c s}, \tag{2}$$

$$\text{MAF}(z) = \frac{1}{\mathscr{T}_d}\frac{1 - z^{-\mathscr{T}_d}}{1 - z^{-1}}, \tag{3}$$

where $\mathscr{T}_c$ is the filter window length in time and $\mathscr{T}_d$ is the corresponding number of discrete samples, which can be obtained as $\mathscr{T}_d = \mathscr{T}_c/\mathscr{T}_s$ with $\mathscr{T}_s$ being the sampling-time used for discrete-time implementation. The MAF can provide complete immunity against nominal frequency odd-order harmonics depending on the considered window length. This has motivated us to consider this PLL. However, it requires an orthogonal signal generator, for which enhanced second-order generalised integrator (E-SOGI) filter is used [34,35]. This filter uses a low-pass filter (LPF) together with the standard SOGI block [36], where the SOGI block generates the quadrature signal and the LPF block is used to eliminate the dc offset. The transfer functions of the E-SOGI filter are given by,

**Table 1**
Circuit and control parameters.

| Symbol | Parameter | Value |
|---|---|---|
| $L$ | Inductor | 1.9mH |
| $r_{sl}$ | Inductor series resistance | 10mΩ |
| $C_0$ | Output capacitor | 747.7$\mu$F |
| $r_{sc}$ | Capacitor series resistance | 1$\mu\Omega$ |
| $R_L$ | Load resistance | 200Ω |
| $V_{dc}$ | DC-link voltage | 400$V$ |
| $f_{sw}$ | PWM frequency | 50KHz |
| $V_{in}$ | Nominal grid voltage (p-p) | 170$V$ |
| $\omega$ | Grid frequency | 50Hz |
| $k_{pv}$ | Voltage proportional gain | 0.115 |
| $k_{iv}$ | Voltage integral gain | 21.75 |
| $k_{pi}$ | Current proportional gain | 0.0933 |
| $k_{ii}$ | Current integral gain | 12.81 |
| $\mathscr{E}_0$, $\mathscr{E}_1$ | Nonlinear function gains | 10, 0.1 |
| $k_s$ | ESOGI gain | 0.8 |
| $\omega_f$ | ESOGI cut-off frequency | 30Hz |
| $k$ | ESOGI PLL gain | 28 |
| $T_{sc}$ | Controller time-step | 10$\mu$sec. |
| $T_s$ | Simulation time-step | 0.667$\mu$sec. |

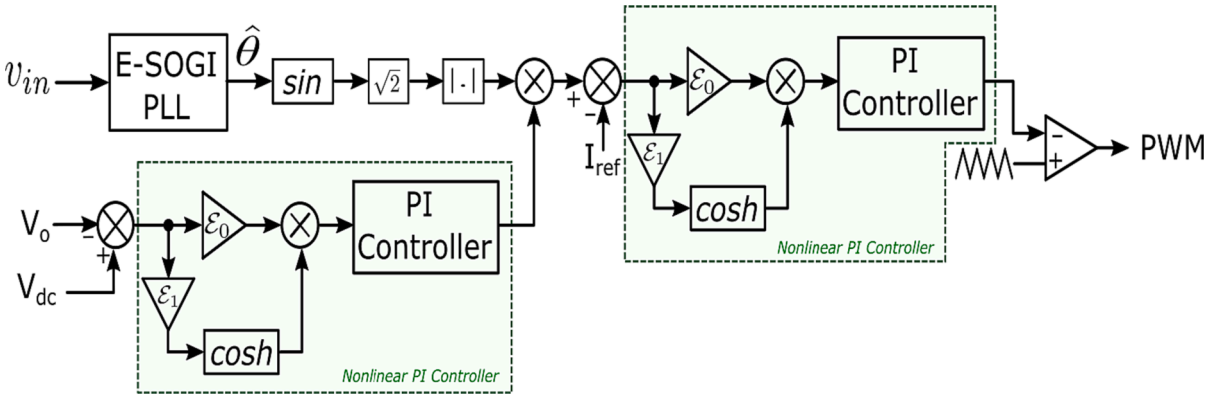


**Figure 8.** Block diagram of the proposed Type IV PI controller.

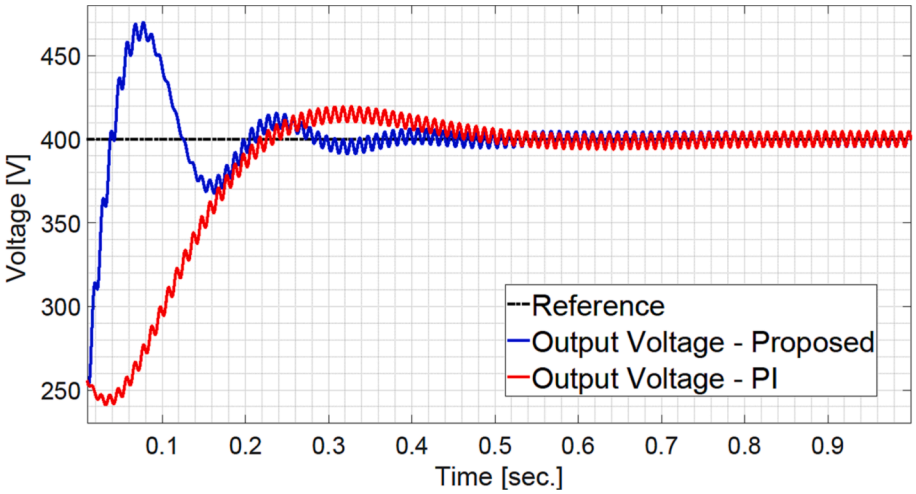


**Figure 9.** Output voltage for the case T1.

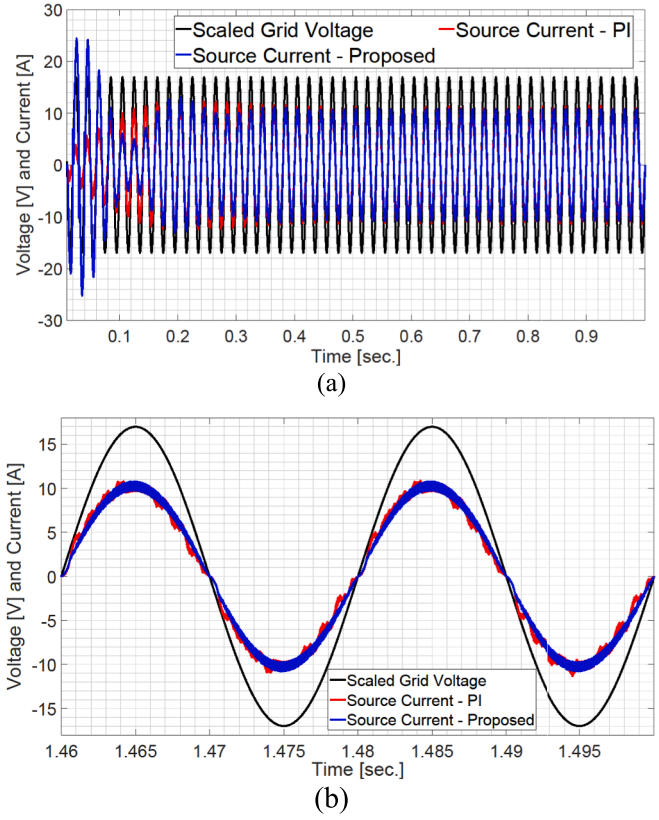


**Figure 10.** Grid voltage (1/10-scaled) and currents for T1: (a) transient responses and (b) zoomed-in steady-state view.

$$\mathscr{G}_{\alpha}(s) = \frac{v_{\alpha}(s)}{v_{in}(s)} = \frac{k_s \widehat{\omega} s}{\mathscr{P}(s)}, \tag{4}$$

$$\mathscr{G}_{\beta}(s) = \frac{v_{\beta}(s)}{v_{in}(s)} = \frac{k_s s(\widehat{\omega}^2 - \omega_f s)}{(s+\omega_f)\mathscr{P}(s)}, \tag{5}$$

where $v_{\alpha}$ and $v_{\beta}$ are the E-SOGI estimated in-phase and quadrature component of the grid voltage signal without any dc offset, $\widehat{\omega}$ is the PLL estimated grid frequency, $k_s > 0$ is the E-SOGI gain, $\omega_f > 0$ is the LPF cut-off frequency, and $\mathscr{P}(s)$ is a polynomial function having the form of $\mathscr{P}(s) = s^2 + k_s \widehat{\omega} s + \widehat{\omega}^2$. The gain $k_s$ determines the selectivity of the

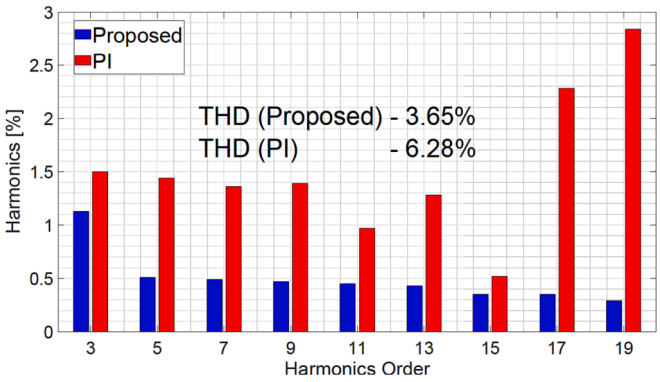


**Figure 11.** Source current THD for case T1.

filter, which can be tuned as a trade-off between harmonic filtering and dynamic performance. A similar trade-off can also be used for the LPF cut-off frequency $\omega_f$ selection. In [34,35], $k_s = 0.8$ and $\omega_f = 30$Hz is selected and the same values are considered here.

The filtered signals $v_{\alpha}$ and $v_{\beta}$ can be used for the conventional QT1-PLL implementation as shown in Fig. 5 (a). QT1-PLL has two parameters, namely the MAF window length and the loop-filter gain $k$. In this work, we are interested in odd-order harmonics reduction, which are also emphasised in the IEEE Std. 519-2014. As such, a window length of $T/2$ ($T$ being the grid voltage nominal period) is considered in this work. To tune the loop-filter gain $\omega_f$, a settling-time-based approach can be considered [37]. For a +1Hz step- change in the frequency, the settling time for the frequency estimation as a function of the gain k can be found in Fig. 6. The results show that $k = 28$ gives the lowest settling-time, which has been selected as the loop-filter gain value.

*Nonlinear PI Control*

Before giving the details of the nonlinear PI controller, let us consider the linear PI controller that is given by:

$$u = \underbrace{(r-y)}_{e}\underbrace{\left(K_p + \int K_i dt\right)}_{PI} \tag{6}$$

where $r$ is the reference, $y$ is the output and $K_p$ and $K_i$ are the proportional and integral gains, respectively. The conventional PI controller uses fixed gains and calculates the control signal by passing the tracking

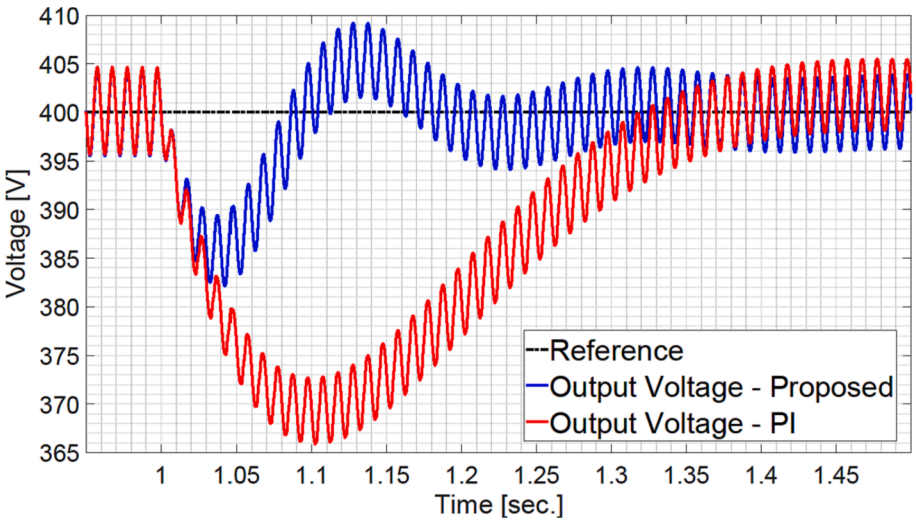


**Figure 12.** Output voltage for the case T2.

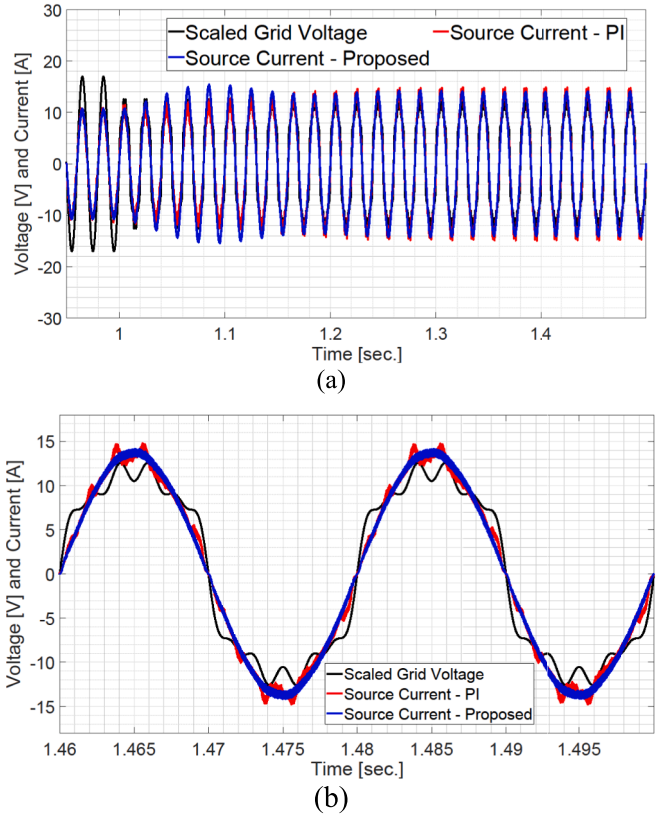


**Figure 13.** Grid voltage (1/10-scaled) and currents for T2: (a) transient and (b) zoomed steady-state view.

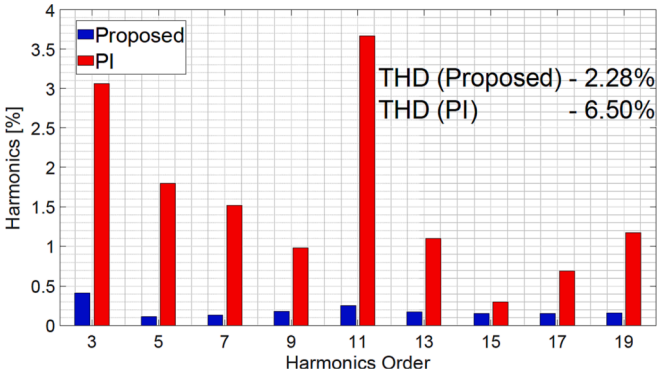


**Figure 14.** Source current THD for case T2.

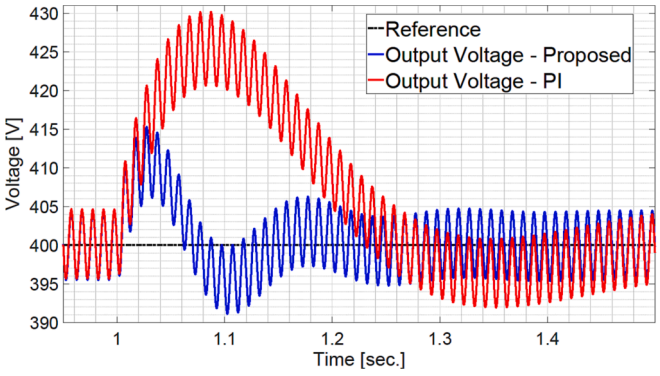


**Figure 15.** Output voltage for the case T3.

error signal $e$ through the proportional and integral part of the controller. There are copious methods [38] to tune the PI controllers, where often there is a trade-off between fast dynamic response and disturbance rejection. In general, a fast dynamic response comes at the cost of disturbance rejection property. The boost PFC converters can have disturbances coming from the grid and the load-side and require a quick response to any change in the system operating condition. The linear PI controllers cannot achieve both of these requirements at the same time. This has motivated researchers to consider nonlinear PI controllers [39,40,41,42,43] for various engineering systems. It has been observed in [42] that nonlinear PI controllers can provide improved tracking accuracy together with enhanced damping and dynamic response. Most of the nonlinear PI controllers available in the literature are typically made of a linear part and a nonlinear part. The linear plant can be designed for the nominal system whereas the nonlinear part will provide additional robustness and dynamic performance improvement. Moreover, although linear approximations are used to model engineering systems, in practice they are often nonlinear in nature due to the presence of parasitic elements, unmodelled dynamics and various nonlinear effects such as backslash, saturation etc. In

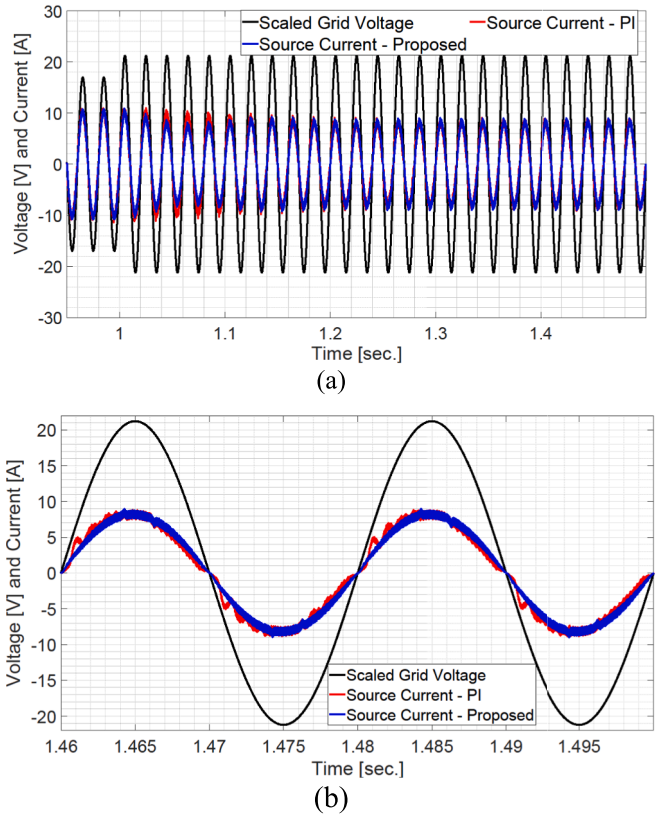


**Figure 16.** Grid voltage (1/10-scaled) and currents for T3: (a) transient and (b) zoomed steady-state view.

this context, nonlinear PI controllers are more suitable to handle inherently nonlinear systems such as the boost PFC converter. In this work, the considered nonlinear PI controller has the following form:

$$u(t) = \varphi(e)\left(K_p + \int K_i dt\right) \tag{7}$$

where the nonlinear function is given by, $\varphi(e) = e\mathscr{E}(e)$, which provides nonlinear modification to the error before passing it to the linear part of the controller. The nonlinear counterpart of the linear PI controller has an additional parameter to tune, which is the nonlinear function $\mathscr{E}(e)$. To ensure fast tracking, this function has to amplify the tracking error when it is far from the equilibrium, whereas the function has to scale down the error when it is near to equilibrium. In other words, this will generate large control action when the tracking error is far from the origin and small control action when the tracking error is near the origin. In addition, the controller value should respect the physical limit of the device to maintain stability. This can be ensured by providing bounded control action. The aforementioned characteristics can be provided if hyperbolic function is selected as follows:

$$\mathscr{E}(e) = \mathscr{E}_0 \cosh(\mathscr{E}_1 e) \tag{8}$$

where $\mathscr{E}_0$ and $\mathscr{E}_1$ are the nonlinear function tuning gains. The considered hyperbolic function is symmetric about the y-axis, which makes sure that the nonlinear function will not change the sign of the error before passing it to the linear part of the controller. In addition, at the origin, this function becomes 1. Therefore, when multiplied by the error itself, the output of nonlinear function $\varphi(e)$ will become 0 as $\varphi(e) = e\mathscr{E}(e)$, which is the same as the actual error. As such, when there is no tracking error, the nonlinear function will generate the same output as the linear error $e$. Error amplification and/or scaling down by the nonlinear function can be observed in Fig. 7, where the output of the nonlinear function (8) for various tracking errors are shown.

This figure shows that as the error moves far from the origin, the output of the nonlinear function increases significantly. However, the opposite effect can be seen when the error is near to the origin. In addition, the gain $\mathscr{E}_0$ can also be used for controlling the gain rate. In general, no specific rules are available for the tuning of the gain $\mathscr{E}_0$ and $\mathscr{E}_1$. As such, a judicious choice has to be made to ensure fast response,

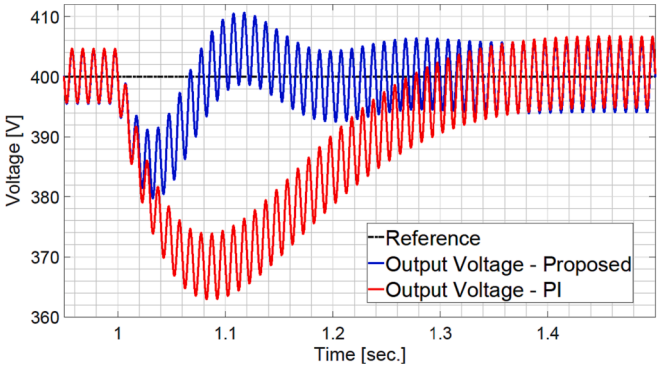


**Figure 18.** Output voltage for the case T4.

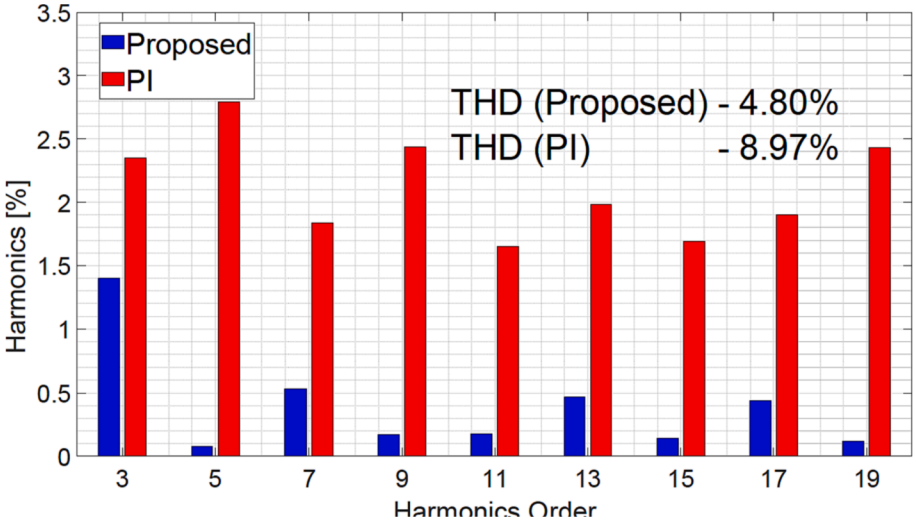


**Figure 17.** Source current THD for case T3.

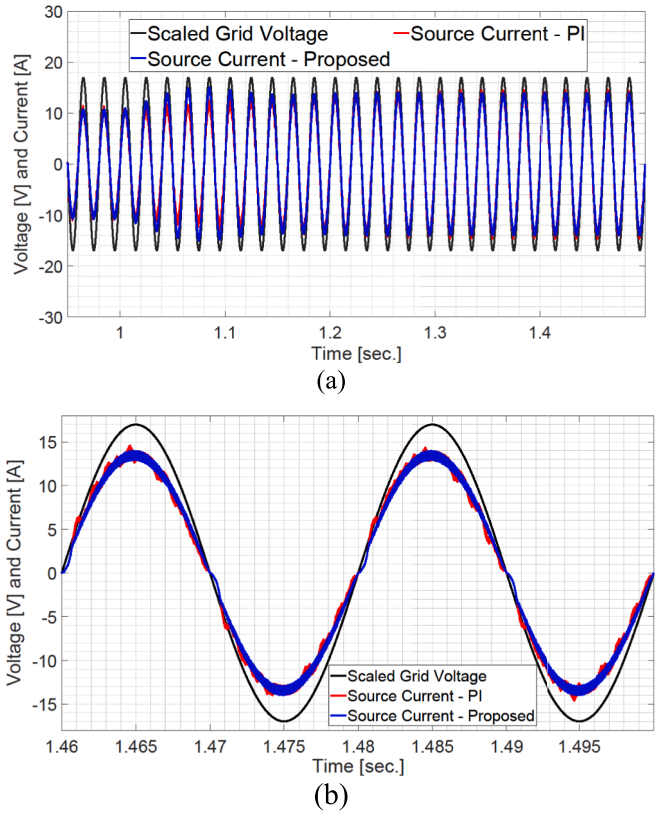


**Figure 19.** Grid voltage (1/10-scaled) and currents for T4: (a) transient and (b) zoomed steady-state view.

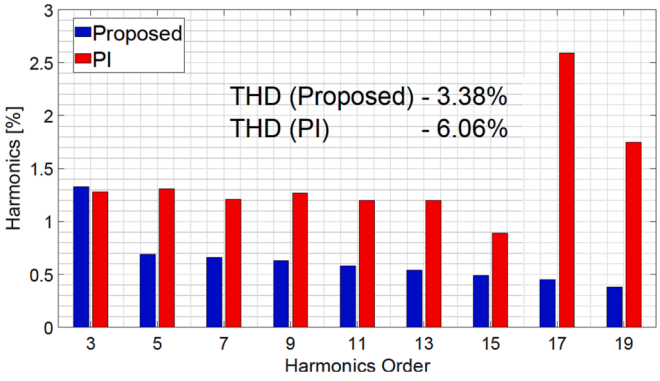


**Figure 20.** Source current THD for case T4.

**Table 2**
A summary of comparative THD.

| Test Case | THD (%) | | Performance Improvement |
|---|---|---|---|
| | Proposed | PI | |
| T1 | 3.65 | 6.28 | ≈ 42% |
| T2 | 2.28 | 6.5 | ≈ 65% |
| T3 | 4.8 | 8.97 | ≈ 47% |
| T4 | 3.36 | 6.06 | ≈ 45% |

good disturbance rejection and system stability. The overall block diagram of the proposed Type IV controller can be found in Fig. 8. Two PI controllers are used here; one in the outer voltage loop and one in the inner current loop. The gains of these controllers are denoted by $k_{pv}, k_{pi}$, $k_{iv}$, and $k_{ii}$, respectively. Interested readers may consult [42] and the references therein for details about the stability analysis of the N-PI controller.

## Results and Discussions

Here, a comprehensive testing of the developed method is considered using numerical simulation through Simulink. The PFC circuit parameters taken from [44], grid detection method and controller gains are given in Table 1. Nonlinear gains of the applied N-PI controller are selected using a trial-and-error method, and the gains of the proposed PLL are selected according to the tuning process given in Sec. 2.1. As a comparison tool, the conventional PI controller (same parameters as listed in Table 1) with E-SOGI-FLL is considered [34,35]. To comprehensively evaluate the performance of the proposed method, the following case studies have been considered:

- T1: Nominal grid voltage and load condition
- T2: Grid voltage sag with harmonic distortion
- T3: Grid voltage swell
- T4: Load change

In analysing the results in this section, the THD will be used as a performance factor similar to the existing literature [45,46] and it is calculated as:

$$\text{THD} = \frac{\sqrt{\sum_{n=2,3,\cdots} I_n^2}}{I_1} \tag{9}$$

where $I$ indicates RMS value of the current and the harmonic and fundamental components of the current are denoted by the subscript 1 and $n$, respectively.

Simulation results for the case T1 are given in Figs. 9-11. The output voltage profiles in Fig. 9 show that the proposed method reaches the steady-state 100 msec earlier than the conventional PI counterpart. The steady-state voltages for the two methods are similar. This indicates the advantage of nonlinear PI over the linear one as the nonlinear function reacts faster when the actual voltage is far from the reference voltage.

The scaled-down grid voltage and source currents drawn by the PFC are given in Fig. 10. The voltage is scaled down for visualisation purpose where the in-phase behaviour of the source current can be shown together with the grid voltage. The steady-state results in Fig. 10(b) show that the current drawn by the proposed method is more sinusoidal compared to the conventional PI controller. This is reflected in the THD plot shown in Fig. 11. Note that in Fig. 11, only odd-order harmonic components distortion are shown as it is the odd-order harmonics that distort the shape of the sinusoid. The THD of our proposed method is approximately 42% lower than the conventional PI method, which highlights the advantage of the proposed method in the nominal voltage condition. This also makes the PFC system with the proposed controller more efficient compared to conventional PI controller.

In the case T2, a sudden grid voltage drop by $-0.25$p.u. is considered. In addition, the $3^{rd}, 5^{th}, 7^{th}$ and $7^{th}$-order harmonics of 0.1p.u., 0.08p.u., 0.06p.u., and 0.05p.u. , respectively, are added. This makes the grid heavily distorted. Simulation results for the case T2 are given in Figs. 12-14. The output voltage profiles in Fig. 12 show that the proposed method reaches the steady-state within 30msec. , whereas for the conventional controller, it takes approximately 50msec. In addition, the peak deviation from the reference 400$V$ is also significantly lower by the proposed method. The steady-sate results in Fig. 13 show that the current drawn by the conventional PI method is more sensitive to the grid voltage distortion unlike the proposed method, which is also evidenced by the THD numbers in Fig. 14. The source current drawn by the proposed method has lower distortion than the conventional counterpart.

In addition to voltage sag, voltage swell may also happen in the grid. In recent times, residential solar photovoltaic (PV) system has started to

**Table 3**
Qualitative comparison of the proposed system with the wider boost PFC control literature.

| Ref. | Sensors | | Controller | | Grid Detection | Dynamic Response | Harmonic Robustness | DC Offset Rejection | Complexity Implementation | Tuning |
|---|---|---|---|---|---|---|---|---|---|---|
| | V | I | V | I | | | | | | |
| [13] | 2 | 2 | PI | SMC | NA | Fast | Low | No | Medium | Medium |
| [21] | 2 | 1 | PI | FLC | NA | Medium | Low | No | Medium | Medium |
| [22] | 2 | 1 | IOL | NA | NA | Slow | Low | No | High | High |
| [23] | 2 | 1 | PI | ADRC | NA | Medium | Low | No | Medium | Medium |
| [24] | 2 | 1 | - | MPC | NA | Medium | Medium | No | Medium | Medium |
| [28] | 2 | 1 | PI-RC | PI | pPLL | Medium | Medium | No | High | High |
| [29] | 2 | 1 | PI | PI | IIR-PLL | Slow | High | No | Low | Low |
| [30] | 2 | 1 | PI | PR | SOGI-PLL | Slow | High | No | High | High |
| Proposed | 2 | 1 | N-PI | N-PI | ESOGI-PLL | Fast | High | Yes | Low | Medium |

NA - Not Applicable

become very popular. It has already been documented in the literature that increase in PV penetration causes over-voltage in the low voltage distribution grid [47].

To assess the effectiveness of the proposed controller to deal with voltage swell, i.e., case T3, a voltage swell of $+0.25$p.u. is considered and the results are given in Figs. 15-17. As shown in Fig. 15, the voltage swell causes sudden deviation of the output voltage and it returns to the steady-state value within 30msec by the proposed method. In the comparison with the conventional controller, the overshoot is almost 100% higher and the steady-state is achieved by 50msec. . These results for case T3 are consistent with the findings of case T2. In the last case, a sudden change in the load has been considered. Initially the load was 200Ω prior a sudden reduction to 150Ω. The results are shown in Fig. 18-20. The output voltage graphs in Fig. 18 shows that the results are consistent with the two previous test cases. As expected, lowering the load value caused an increase in the source current shown in Fig. 19. Higher current caused an improvement in the THD profile as shown in Fig. 20. This figure also highlights the performance improvement by the proposed method even when the load value reduces. The comprehensive performance evaluation through case studies T1-T4 show that the proposed method is highly robust to grid voltage distortion, and can accommodate quickly any change in the operating conditions e.g., voltage and load, and, provides very low THD *cf.* Table 2. A qualitative comparison of the proposed method over the wider literature is shown in Table 3. This table shows that compared to the existing alternatives, the proposed method offers several competitive features and performance improvement, which makes the proposed method very suitable for PFC converters.

In the smart farming case, the natural day-night cycle is emulated by the LED lights. Often a longer day is preferred for plant growth [4]. This requires the LED lights to be on for a long time and without any interruption. As such, having a lower THD will make the overall system more efficient as it will draw less current from the grid. In addition, lower THD also makes the smart farming grid-friendly.

It is well known that higher THD causes heating and other issues in the load. So, lowering the THD will also improve the lifetime of the LED system (driver and light), thereby making the system more economical to operate. This may further accelerate the growth of smart-farming as an alternative to conventional farming practice.

## Conclusion

This paper studied the control of boost PFC converters in the context of smart farming. The proposed controller consists of an advanced grid-detection scheme and nonlinear PI scheme. The idea behind the nonlinear PI scheme is well detailed and a step-by-step development and tuning of the proposed PLL are given. The results from several case studies show that the proposed method outperformed the conventional counterpart in terms of 42% $\sim$ 65% reduction in THDs and smaller settling time. Therefore, the proposed controller can enhance the efficiency of the boost PFC converter, which will lower the operational cost of the converter used in smart farming applications. This will further accelerate the growth of smart farming as a cost competitive alternative to conventional farming.

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## Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

## Data availability

No data was used for the research described in the article.

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