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Inverter with Paralleled-Modules to Extend Current Capacity and Combat Motor Overvoltage in SiC-Based Adjustable Speed Drives

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***Abstract*—This article proposes a quasi-three-level (Q3L) PWM-based module-parallel inverter to address two major issues of deploying SiC MOSFETs in high-power cable-fed adjustable speed drives. Firstly, the maximum output power of SiC inverters is limited due to the lack of high current rating SiC devices, which cannot satisfy the demand of high-power applications such as heavy-duty electric vehicles and more electric aeroplanes. The second issue comes from the fast-switching speed of SiC MOSFETs, where power cables act like transmission lines under steep rising/falling voltages (high dv/dt), with back and forth voltage reflections that result in serious overvoltage oscillations at motor terminals. To address these issues, a SiC module-parallel inverter is adopted with elevated current capacity, where the phase voltage is maintained at the mid-point of a coupled inductor connected to the output nodes of each paralleled half-bridge module. By actively controlling the switching delay between the paralleled half-bridge-legs, Q3L PWM waveforms are generated at the inverter output nodes which can mitigate the motor overvoltage due to the voltage reflections through power cables. An active current control technique is also proposed to facilitate the current balance between the paralleled half-bridge-legs. The proposed Q3L PWM-based module-parallel inverter is experimentally verified using a SiC-based cable-fed motor drive system. The results show that the proposed approach can extend the current capabilities of SiC devices as well as mitigate the motor overvoltage, enabling the adoption of SiC devices in high-power motor drives.**

***Index Terms*—Adjustable speed drives, coupled inductor, high dv/dt, motor overvoltage, parallel, SiC MOSFETs, reflected wave phenomenon.**

I. Introduction

Power density, efficiency and reliability are key design drivers and central concerns for adjustable speed drives in a range of applications including industrial automation and robotics, transportation and renewable energy systems. Wide bandgap (WBG) power semiconductor devices such as silicon carbide (SiC) MOSFETs offer significant potential for improving the power density and efficiency of adjustable speed drives due to their superior material characteristics [1]–[4]. For instance, SiC MOSFETs can operate at higher switching frequencies while maintaining high efficiency due to their fast-switching speed, compared with silicon (Si) IGBTs, which reduces passive filtering components and cooling requirements [5]–[7]. Consequently, SiC MOSFETs offer a promising alternative to Si IGBTs in adjustable speed drives for a wide range of applications, where they are becoming more competitive on energy saving, power density improvement, and system-level cost reduction [1].

However, the application of SiC MOSFETs in adjustable speed drives is also facing several issues [8], to fully realize their potential [1]. Among them, there are two major challenges of adopting SiC MOSFETs in high-power adjustable speed drives, i.e., the maximum output power limitation of the inverters [9] and the serious transient overvoltage at motor terminals [10].

The first challenge is due to the lack of high current rating SiC switching devices [11]. With wider electrification in high power applications, inverters with high power ratings are necessary. For example, inverters in the power range of 100-500kW for heavy duty electric vehicles [12] and megawatts-level power inverters for more/all electric aircrafts [13]–[15] are highly demanded. Due to the limited current rating of SiC chips, parallel connection of SiC MOSFETs can be an approach to improve the current capacity of switching devices [11]. Furthermore, parallel connection of switching devices is also a cost-effective approach even in low power applications since the high-current devices are generally more expensive than equivalently rated parallel-connected low-current counterparts. For example, at the time of writing, the Wolfspeed C3M0016120D SiC MOSFET (1200V/115A, $70.4) is 37% more expensive than two C3M0032120D (1200V/62A, $ 25.7) low current ones [16]. However, paralleling SiC devices is a challenging approach due to potential current imbalance among paralleled SiC MOSFETs [11]. Owing to the unavoidable switching time mismatch and/or characteristic difference among the paralleled devices, both the steady-state and transient currents may not be equally shared among the devices, resulting in overcurrent and overtemperature in some devices [17]. This adversely affects the inverter reliability and limits the usable current rating of the

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devices. Therefore, several approaches have been proposed to overcome the current imbalance among the switching devices [17]. For example, [18] uses active gate drivers to handle the imbalance current. However, these gate drivers require high-bandwidth current sensors and feedback control, which increases the implementation complexity. Moreover, paralleling multi-chips also poses challenges on the gate driver design, where a very-high current output capability is required to drive the paralleled chips to achieve simultaneous turn-ON and turn-OFF while providing a very fast switching speed [9].

The second challenge comes from the fast voltage transients (high dv/dt) of inverter output voltages due to the fast-switching speed of SiC MOSFETs [10]. In a typical SiC cable-fed motor drive system, as shown in Fig. 1, the fast-fronted voltage transients make the power cables act like transmission lines, where the waves travel along the cable forward and backward [10]. Due to the characteristic impedance mismatch between the cable and motor, the voltage pulses are reflected at motor terminals, resulting in serious overvoltage which can be double the inverter voltage [19]. This is known as the reflected wave phenomenon [20]. The resultant overvoltage due to the reflected wave phenomenon depends on the employed cable length, rise and fall times of PWM voltage pulses, and characteristic impedances of the cable and motor [21]. With shorter switching rise/fall times of SiC MOSFETs, the overvoltage at motor terminals is more common and severe in SiC adjustable speed drives compared with Si counterparts, where the voltage at the motor terminals can be twice the inverter voltage with few meters of cable [22]. In addition to the fast-switching speed, the higher switching frequency of SiC power inverters brings new issues for the adjustable speed drives, i.e., the double pulsing effects, where the motor may experience more than twice the inverter voltage due to the addition of reflected voltage pulses [10]. The resultant overvoltage stress at motor terminals adversely affects the lifetime of motor winding insulation through the inception of partial discharges that progressively yield to the degradation and premature failure of organic coatings of motor coils [23]. This significantly affects the reliability and lifetime of adjustable speed drives.

Several approaches have been investigated in literature to attenuate the overvoltage oscillations at motor terminals in cable-fed motor drive systems [21], [22], [24]–[28]. In [21] the voltage slew rate is actively shaped using a SiC soft-switching inverter, as shown in Fig. 2a, to mitigate the motor overvoltage as well as reduce the switching loss. [22] and [25] adopt a T-type inverter, as shown in Fig. 2b, to generate a quasi-three-level (Q3L) voltage waveform to cancel out the motor overvoltage oscillations. [26]–[28] further develop the Q3L PWM concept by using new circuit topologies. However, these approaches cannot be employed in high power applications due to the lack of high current rating SiC devices.

This article aims to tackle the aforementioned two issues of deploying SiC MOSFETs in high power adjustable speed drives. **The main contributions of this article are summarized as follows:** A Q3L PWM-based module-parallel inverter, as shown in Fig. 3, is proposed to elevate the current capacity and mitigate the motor overvoltage in SiC-based adjustable-speed drives. The motor overvoltage mitigation mechanism of the proposed PWM scheme is mathematically

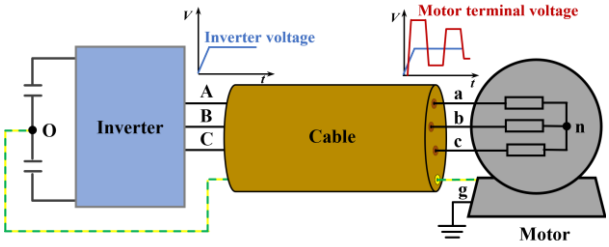


Fig. 1. A typical cable-fed adjustable speed drive system.

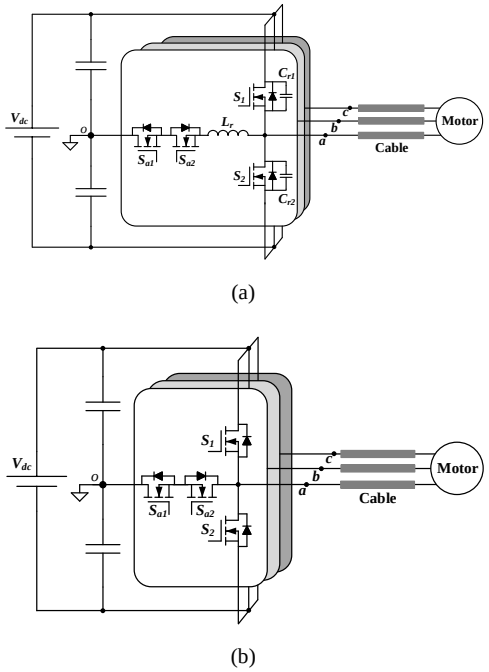


Fig. 2. Inverter topologies for motor overvoltage mitigation in cable-fed motor drives (a) Soft-switching inverter [21] and (b) T-type inverter [22] and [25].

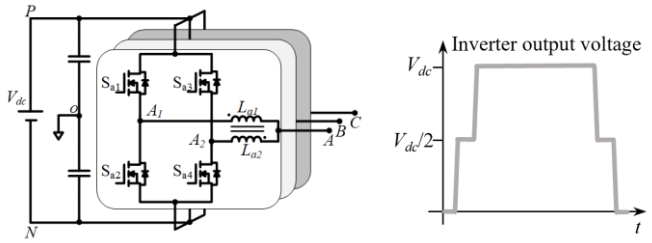


Fig. 3. A three-phase SiC Q3L PWM-based module-parallel power inverter.

derived in both time and frequency domains. In addition, to facilitate the current balance between the parallel-connected modules, an active current control technique is proposed.

The rest of this article is structured as follows. Section II provides brief modelling of the voltage reflection phenomenon in adjustable-speed drives and analyses the Q3L overvoltage mitigation mechanism in the time domain and frequency domain. In section III, the proposed Q3L PWM-based module-parallel inverter is presented and its operation principles are illustrated. Section IV provides experimental verification of the proposed approach. Finally, conclusions are drawn in Section V.

II. Reflected Wave Phenomenon and Q3L Mitigation Mechanism

A. Modeling of reflected wave phenomenon

In SiC adjustable-speed drives, the fast-switching PWM pulses are reflected at the motor terminals due to the impedance mismatch between the power cable and motor, resulting in excessive motor overvoltage oscillations. Several models have been presented in literature to investigate the reflected wave phenomenon. For example, [21] uses a bounce diagram to graphically illustrate the voltage reflection mechanism. Fig. 4 depicts the inverter voltage V_s and motor terminal voltage V_m in a cable-fed motor drive system, where V_{dc} is the dc-link voltage, t_p is the wave propagation time in the power cable from one end to the other, Γ_m and Γ_s are the reflection coefficients at the motor and inverter terminals, respectively.

Referring to Fig. 4, the maximum overvoltage at the motor terminals can be given as [21]:

$$V_m = (1 + \Gamma_m)V_{dc} \tag{1}$$

where, Γ_m is calculated in terms of the characteristic impedance of cable Z_c and motor Z_m, as [21]:

$$\Gamma_m = \frac{Z_m - Z_c}{Z_m + Z_c} \tag{2}$$

Typically, $Z_m \gg Z_c$ which results in $\Gamma_m = 1$, implying the voltage is fully reflected at the motor side.

The overvoltage oscillation frequency f_{rw} can be expressed as [21]:

$$f_{rw} = 1/4t_p \tag{3}$$

where, the propagation time t_p depends on the adopted cable length l_c, and the per-unit length inductance L_c and capacitance C_c, as [21]:

$$t_p = l_c\sqrt{L_c C_c} \tag{4}$$

B. Q3L overvoltage mitigation mechanism in time domain

If the inverter output voltage V_s is reshaped as a Q3L waveform, where the rising edge is split into two identical voltage steps (V_{s1} and V_{s2}) with a proper dwell time t_{dwell}, the motor overvoltage can be significantly attenuated, as elucidated in Fig. 5. The amplitudes of V_{s1} and V_{s2} are $\frac{V_{dc}}{2}$. V_s is given by:

$$V_s = V_{s1} + V_{s2} \tag{5}$$

Referring to Fig. 5, the two voltage steps V_{s1} and V_{s2} experience voltage reflections while traveling from the inverter to the motor across the cable due to the impedance mismatch between the cable and the motor. Note that the reflection coefficients at the inverter and motor sides are assumed to be unity. V_{m1} and V_{m2} are the reflected voltages of V_{s1} and V_{s2}, where they both have an amplitude of V_{dc}. Accordingly, the resultant motor voltage V_m can be given as:

$$V_m = V_{m1} + V_{m2} \tag{6}$$

If V_{s2} lags V_{s1} by $t_{dwell} = 2t_p$, the overvoltage oscillations of V_{m1} and V_{m2} can be fully counterbalanced, as shown in Fig. 5. Thus, the motor overvoltage can be significantly mitigated.

In a similar mitigation mechanism, if the falling edges are shaped as a Q3L waveform with a dwell time $t_{dwell} = 2t_p$, the motor will not experience overvoltage oscillations at the falling switching transitions either.

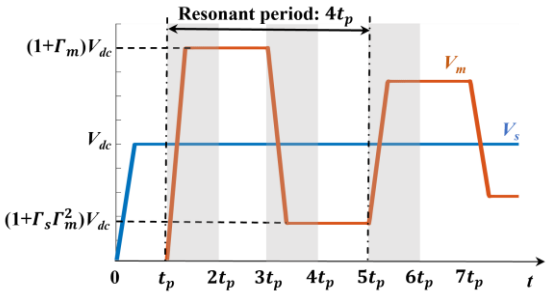


Fig. 4. Inverter voltage V_s and motor terminal voltage V_m in cable-fed motor drive system.

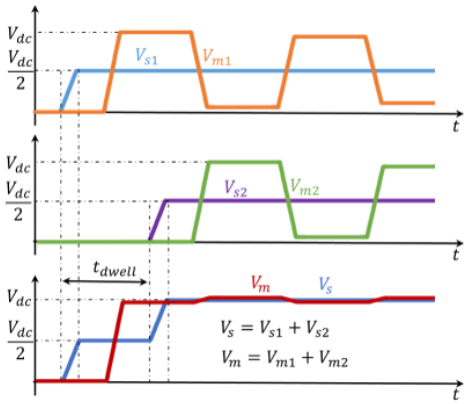


Fig. 5. Overvoltage mitigation mechanism when the voltage is shaped as a Q3L.

C. Q3L overvoltage mitigation mechanism in frequency domain

The Q3L overvoltage mitigation approach can be further analyzed in the frequency domain. Since the Q3L voltage V_s is composed by the two identical voltage steps V_{s1} and V_{s2} with an intermediate dwell time, the inverter output voltage V_s can be represented by the pulse-train shown in Fig. 6.

Referring to Fig. 6, $A/2$ is the pulse voltage amplitude, τ is the average pulse width measured at half the pulse amplitude, T is the fundamental cycle time, and t_r and t_f are the pulse rise and fall times, respectively. For simplicity, the waveform is assumed to be symmetrical (i.e., $t_r = t_f$) with a constant duty ratio ($d = \tau/T$).

According to Fourier analysis, the pulse-train V_{s1} shown in Fig. 6 can be expressed as [29]:

$$V_{s1}(t) = \sum_{n=-\infty}^{n=\infty} c_{n1} e^{jn\omega t} \tag{7}$$

where ω is the angular frequency of the waveform and c_{n1} is the Fourier series coefficient, given as:

$$c_{n1} = \frac{Ad}{2}\,\mathrm{sinc}\left(\frac{n\omega\tau}{2}\right)\mathrm{sinc}\left(\frac{n\omega t_r}{2}\right)e^{-jn\omega\left(\frac{\tau+t_r}{2}\right)} \tag{8}$$

Since V_{s2} lags V_{s1} by t_{dwell}, the Fourier series expansion of V_{s2} can be expressed as:

$$V_{s2}(t) = V_{s1}(t + t_{dwell}) = \sum_{n=-\infty}^{n=\infty} c_{n1} e^{jn\omega(t+t_{dwell})} \tag{9}$$

Substituting (8) and (9) into (5), the Fourier series expression of V_s is:

$$V_s(t) = \sum_{n=-\infty}^{n=\infty} c_n e^{jn\omega t} \tag{10}$$

where, c_n is the Fourier series coefficient, given as:

$$c_n = \frac{Ad}{2}\text{sinc}\left(\frac{n\omega\tau}{2}\right)\text{sinc}\left(\frac{n\omega t_r}{2}\right)e^{-jn\omega\left(\frac{\tau+t_r}{2}\right)}(1+e^{jn\omega t_{dwell}}) \quad (11)$$

At the antiresonance frequency of the motor drive system (i.e., $\omega = 2\pi f_{rw}$), the Fourier series coefficient is:

$$c_n = \frac{Ad}{2}\text{sinc}(n\pi f_{rw}\tau)\,\text{sinc}(n\pi f_{rw}t_r)\,e^{-jn\pi f_{rw}(\tau+t_r)}(1 + e^{j2n\pi f_{rw}t_{dwell}}) \quad (12)$$

From (12), it can be derived that when $t_{dwell} = \frac{1}{2f_{rw}} = 2t_p$, $c_n = 0$, that is, the motor overvoltage can be ideally eliminated since the voltage component exciting the resonance is zero.

III. Q3L PWM for Module-Parallel Inverter

The Q3L voltage pulse-train shown in Fig. 6 can be generated using the module-parallel power inverter by actively controlling the switching delay between the paralleled modules.

A. Module-parallel power inverter

Referring to the circuit schematic shown in Fig. 3, each phase of the module-parallel power inverter consists of two half-bridge-legs connected using two identical inductors. This inverter can be further extended to multiple legs paralleled inverter depending on the switching devices' current rating and the required power level. For simplicity, the two half-bridge-leg paralleled inverter shown in Fig. 3 is considered in this article. Note that the inductors can be either coupled or uncoupled. The coupled inductor with self-inductance L is employed herein because it can significantly reduce the core loss and size, compared with the uncoupled one.

B. Implementation of Q3L PWM

Referring to Fig. 3, the inverter output voltage V_{XN} ($X = A, B, or\ C$) is pertinent to the output voltages of half-bridge-legs X_1 and X_2 (V_{X1N} and V_{X2N}), as:

$$V_{XN} = \frac{V_{X1N} + V_{X2N}}{2} \quad (13)$$

Accordingly, the Q3L PWM voltage can be obtained by inserting a time shift t_{dwell} between the output voltages of the paralleled legs (X_1 and X_2).

Fig. 7 illustrates the gate signal generation for the switching devices in phase A, where the reference modulation signal u_{ref} is compared with two identical triangular carrier signals but shifted by t_{dwell}. Fig. 8 describes the detailed switching transitions considering the devices' parasitic elements when the output current is positive, where Figs. 8a-8e illustrate the commutation process of the output voltage when rising from 0 to V_{dc}, while Figs. 8f-8j illustrate the commutation process of the output voltage when falling from V_{dc} to 0. The corresponding voltage and current waveforms for these commutation processes are shown in Fig. 9. The phase current i_A is assumed to be equally split among the paralleled legs (A_1 and A_2) when the commutation starts.

It is worth noting that for a single half-bridge-leg, the commutation process for the output voltage traversing from 0 to V_{dc} is governed by the gate resistance of the adopted gate driver, while the commutation process of the output voltage from V_{dc} to 0 is governed by the load current and parasitic elements [30]. Referring to Figs. 8a-8c, the output voltage V_{A1N}

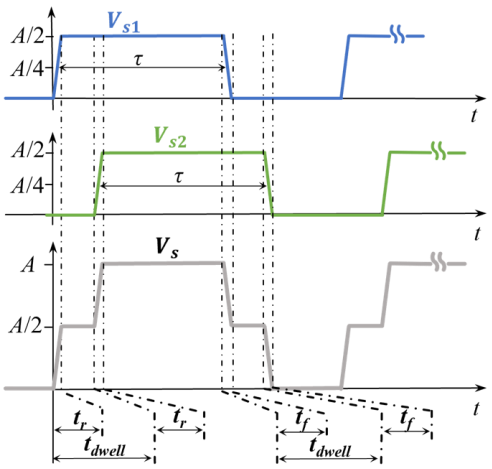


Fig. 6. Q3L pulse-train.

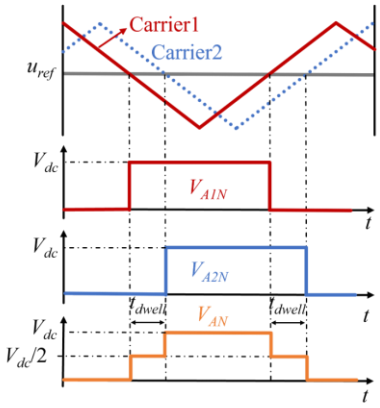


Fig. 7. Q3L wave generation for module parallel power inverter.

swings from zero to V_{dc} when the turn-ON gate signal is applied to the top switch S_{a1} at t_2. Therefore, the output voltage V_{A1N} is denoted by the steep rising edge, as shown in Fig. 9. According to (13), the inverter output voltage V_{AN} becomes $V_{dc}/2$ with halved voltage slew rate. Meanwhile, the inductor currents i_{La1} and i_{La2} start to increase and decrease, respectively, with the same current slew rate, as:

$$\frac{di_{La1}}{dt} = -\frac{di_{La2}}{dt} = \frac{V_{dc}}{2L} \quad (14)$$

The same commutation processes are applicable to the half-bridge-leg A_2, as shown in Figs. 8d and 8e. The output voltage V_{A2N} starts to increase from 0 to V_{dc} when the turn-ON signal is applied to S_{a3} at t_5, as shown in Figs. 8d and 9. According to (13), the inverter output voltage V_{AN} traverses from $V_{dc}/2$ to V_{dc}, as shown in Fig. 9. Then, the inductor current keeps fixed since the voltage across the inductors is zero. The duration of the intermediate voltage level of the inverter output voltage V_{AN} depends on the time delay between the gate signals for legs A_1 and A_2. Referring to Fig. 9, the current difference between the half-bridge-legs is denoted as the offset current I_{offset}, as:

$$I_{offset} = i_{La1} - i_{La2} = \frac{V_{dc}t_{dwell}}{L} \quad (15)$$

Figs. 8f and 8h show the commutation process for leg A_1 from the top switch to the bottom switch. Since the commutation is affected by the load current and parasitic

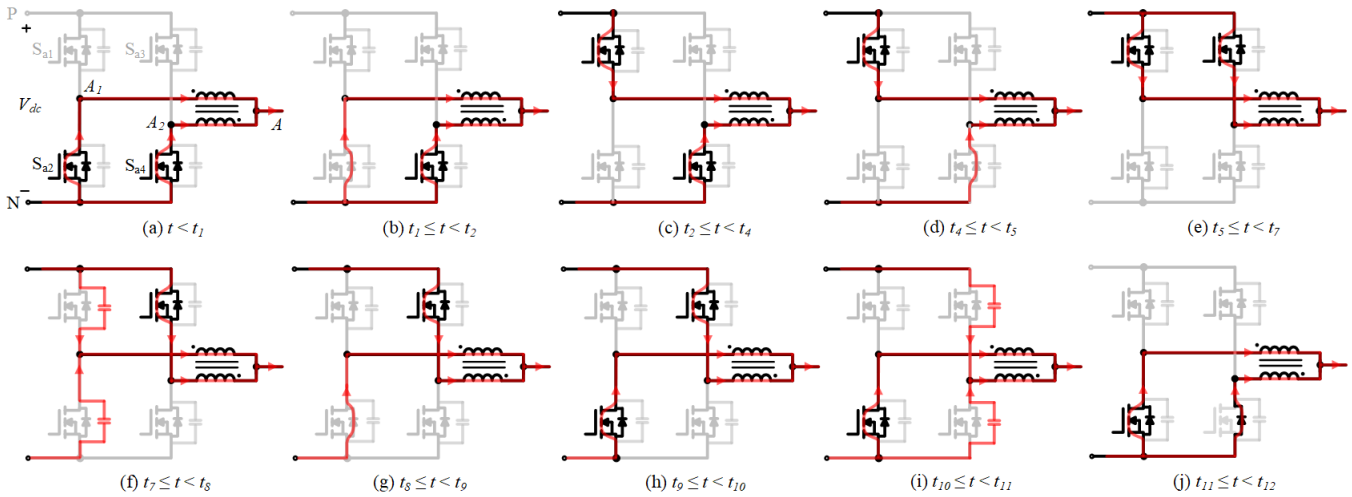


Fig. 8. Switching transitions when phase current is positive.

elements of the devices, the voltage V_{A1N} tardily decreases in a linear manner within a falling time t_{fall}, as show in Fig. 9. t_{fall} is given by [30]:

$$t_{fall} = \frac{2C_{oss}V_{dc}}{i_{load}} \tag{16}$$

where, C_{oss} is the output capacitance of SiC MOSFETs.

The output voltage V_{A1N} keeps $V_{dc}/2$ after the current fully traverses to the bottom switch S_{a2}. Meanwhile, the inductor current i_{La1} decreases and i_{La2} increases, respectively, with the same current slew rate as (14). After a dwell time t_{dwell}, the same commutation processes are applied to leg A_2, resulting in the output voltage traverses from $V_{dc}/2$ to zero, as shown in Figs. 8i and 8j. After that, the inverter outputs zero voltage and the currents flow through the coupled inductor resume the same again, as shown in Fig. 9.

C. *Active current balance control approach*

Referring to Fig. 9, the current flows through leg A_1 is higher than that of leg A_2 during the switching transient, resulting in higher power loss and temperature rise in leg A_1 than A_2. Besides, due to inevitable mismatch among the devices' characteristic, the current flowing through the two half-bridge-legs would be unequal at the steady state, resulting in different steady state loss and temperature rise among the legs. The above issues would result in inductor core saturation and thermal unbalance among the switching devices reducing the usable current rating of the devices. Therefore, the current sharing among the bridge-legs should be actively controlled.

The flow chart in Fig. 10 outlines the proposed active current balance approach for phase A, which involves measuring the inductor currents i_{LA1} and i_{LA2} and accordingly determines which bridge-leg is triggered first during switching. For example, if $i_{LA1} > i_{LA2}$, the bridge-leg A2 will be switched first, otherwise, bridge-leg A1 will be switched first. As the sample and update frequencies are equal to the switching frequency, the currents for each bridge-leg can be actively balanced at the switching frequency. With this approach, the switching devices in the bridge-legs will have equal RMS current value, resulting in the same temperatures.

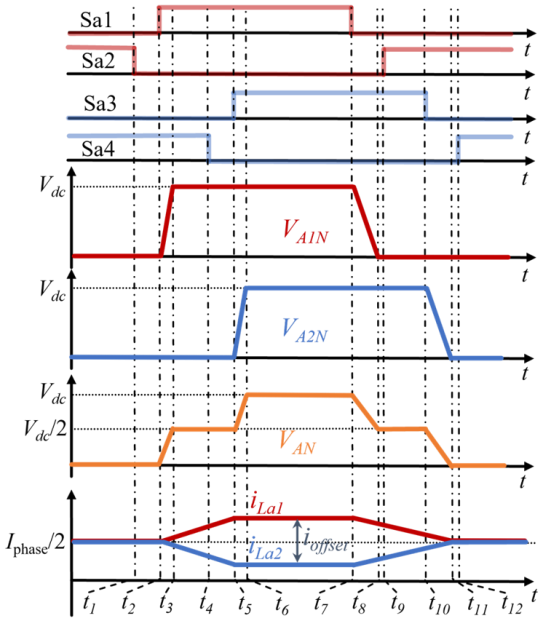


Fig. 9. The gate signals, the output voltages, currents for bridge-legs (A1 and A2), and the inverter output voltage during switching transitions.

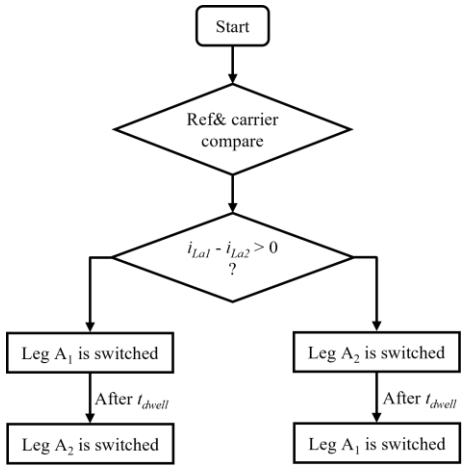


Fig. 10. Flow chart for active current control.

D. *Impact of inductance and cable length on the offset current among bridge-legs*

Fig. 11. shows the offset current I_{offset} with respect to the coupled inductance at different cable lengths, where the dc-link is 400V and the wave propagation time is assumed to be 5.22ns per cable meter [31]. The dwell time is changed according to the employed cable length. Referring to Fig. 11, the offset current increases with the cable length but decreases with the employed coupled inductance, which can be explained using (15).

E. *Impact of duty cycle*

Referring to Fig. 7, the module-parallel inverter can generate the Q3L PWM voltage waveform under normal conditions, which can effectively mitigate the overvoltage at motor terminals in cable-fed motor drives. Under very low duty cycle modulation, as shown in Fig. 12, the inverter generates two consecutive voltage pulses separated by t_{dwell}, with amplitudes of $V_{dc}/2$. Even when the motor is supplied by these voltage waveforms, the maximum voltage at the motor terminals remains within $2 * V_{dc}/2 = V_{dc}$, i.e., twice the incident voltage. Therefore, the proposed approach can effectively mitigate motor terminal overvoltage under both normal and low duty cycles, i.e., the proposed approach has no minimum duty cycle limitation.

IV. Experimental Results

In order to verify the proposed approach, a three-phase module-parallel power inverter based on SiC MOSFETs is built to supply a three-phase induction motor through 12.5 m, four core, 13 AWG long cable, as shown in Fig. 13. Three coupled inductors with 15μH self-inductance are employed. Note that in order to reduce the core loss and keep the same inductance among the bridge-legs, the coupled inductor with bifilar winding structure is used. Fig. 14 shows the schematic and photo of the employed coupled inductor. The SiC power inverter is controlled by the Q3L PWM scheme with $t_{dwell} = 2t_p$. Note that the wave propagation time t_p can be obtained using the offline methods that presented in [21]. Table I shows the main parameters of the experimental setup.

Table I. Experimental Prototype Parameters

	Parameter	Value
Power converter	DC link voltage	400V
	Switching device	C2M0040120D
	Gate resistance	20Ω
	Switching frequency	20kHz
	Fundamental frequency	25Hz
	Dwell time	180ns
	Modulation technique	Q3L PWM
Coupled Inductor	Self-inductance	15μH
	Current rating	25A
Cable	Type	Four-core PVC
	Length	12.5m
	Cable gauge	13AWG
Motor	Type	Induction motor
	Phase number	3
	Pole number	6
	Power rating	2.2kW
Controller	DSP	TI TMS320F28335
	FPGA	XILINX XC3S400

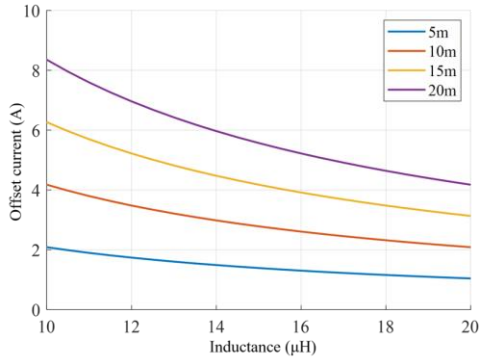


Fig. 11. Offset current with respect to the inductance and cable length when the dc-link voltage is 400V in the Q3L PWM-based module-parallel inverter.

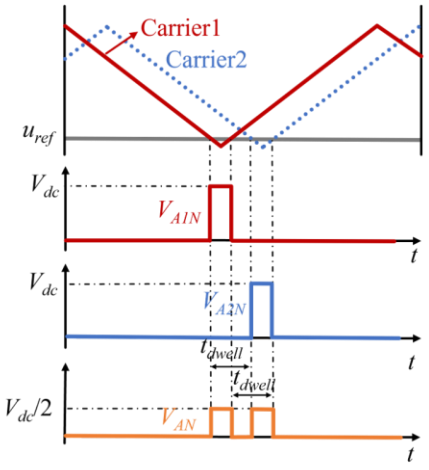


Fig. 12. The output voltage of the module-parallel inverter under very low modulation index.

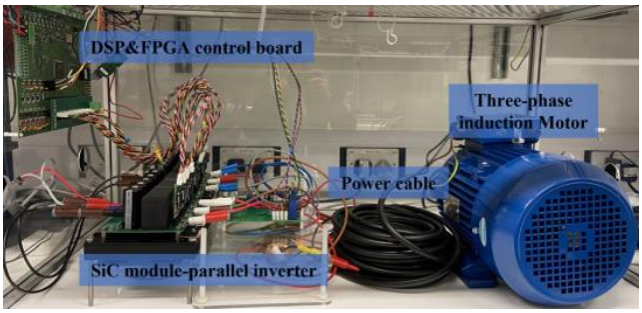
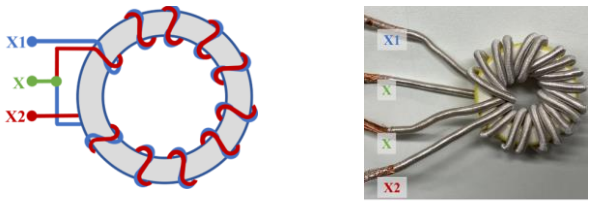


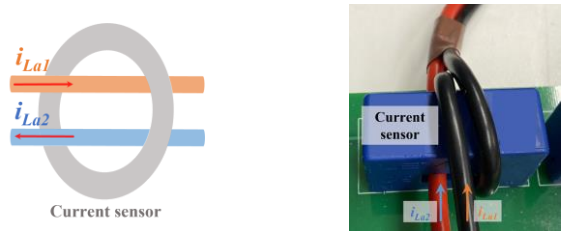
Fig. 13. The experimental setup.



(a) (b)

Fig. 14. (a) schematic and (b) photo of the coupled inductor using the bifilar winding pattern.

Figs. 15a and 15b show the schematic and photo of current measurement circuit for phase A. As shown, the differential



(a) (b)

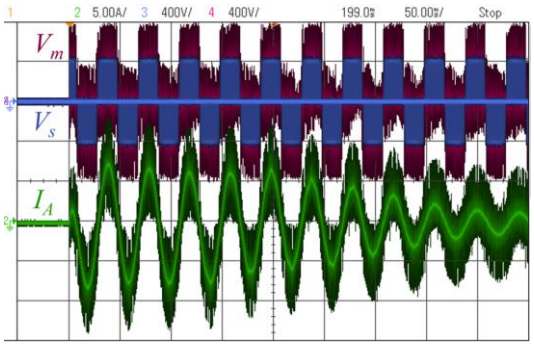
Fig. 15. (a) schematic and (b) photo of the current measurement circuit for one phase.

current of legs A_1 and A_2 is measured using one current sensor, where the obtained differential current is fed into the control board for the active current balance control. This current measurement approach can reduce the number of current sensors from six to three for the three-phase module-parallel power inverter.

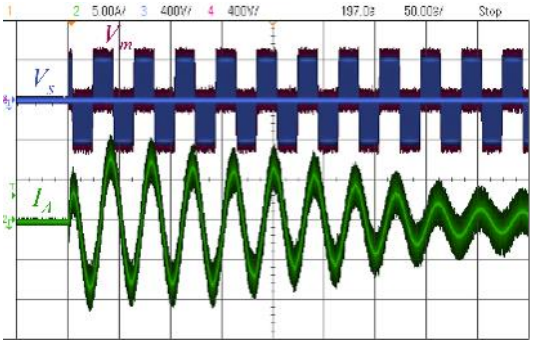
Fig. 16 shows the inverter line voltage V_s, corresponding voltage at motor terminals V_m and the inverter output phase current for motor startup experiment, where Figs. 16a and 16b show the results when the motor is supplied by a two-level (2L) converter and the proposed Q3L module-parallel inverter, respectively. As can be noticed in Fig. 16a, a significant overvoltage at the motor terminals, which is about 2.0 p.u., exists across the motor terminals when the motor is supplied by the conventional two-level inverter. In contrast, the motor overvoltage is significantly mitigated when the proposed Q3L scheme is used, where the peak voltage is about 1.2pu, as shown in Fig. 16b. In addition, there are high frequency spikes in the inverter output current for the 2L inverter. This high-frequency harmonics of the current are due to the high dv/dt charging and discharging the cable parasitic capacitance, along with voltage reflections across the cable. In contrast, the module parallel power converter has cleaner output current waveform than that of the 2L inverter. This returns to the overvoltage mitigation ability of the proposed module-parallel inverter in addition to the attenuated dv/dt of its output voltage which is half that of the 2L inverter. This effectively suppresses the high frequency current spikes.

Fig. 17 shows the experimental results for steady state operation of the motor where Fig. 17a and 17b show the results when the motor is supplied by a 2L converter and the module-parallel inverter, respectively. The results demonstrate that the module-parallel inverter effectively reduces overvoltage at the motor terminals and has a cleaner output current waveform compared to the two-level inverter. In addition, the proposed modulation scheme has a minor impact on the dc-link capacitor's current ripple, given that the dwell time is typically in the nano- to micro-second range. This is demonstrated in Fig. 17, where the dc-link current ripple is 1.8A and 2.0A for the 2L inverter and the module-parallel inverter, respectively.

Fig. 18 shows a comparison between the 2L converter and the module-parallel power inverter in terms of their current frequency response, where Fig. 18a and 18b show the frequency spectrum and THD of the inverter output current, respectively. The results show that the module-parallel inverter effectively reduces high frequency harmonics and achieves a lower THD than the 2L inverter.

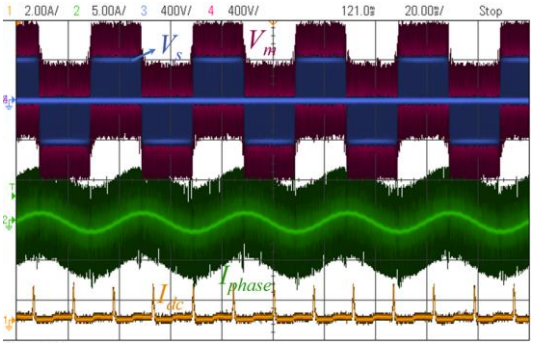


(a)

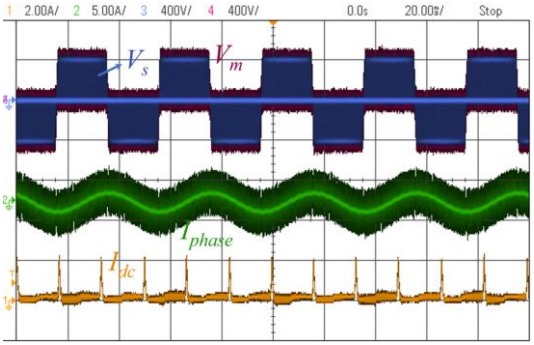


(b)

Fig. 16. Experimental waveforms of inverter line voltage V_s and the motor terminal voltage V_m for motor startup experiment when the motor is supplied by (a) the two-level inverter and (b) the module-parallel inverter.

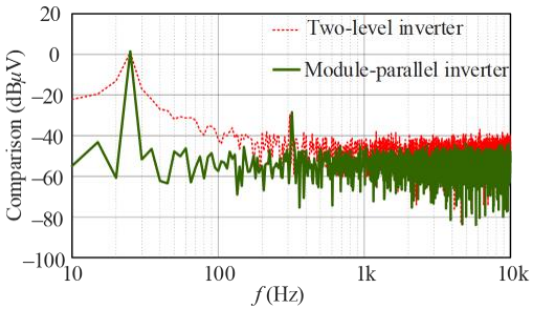


(a)

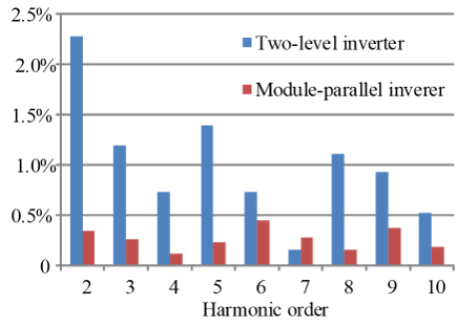


(b)

Fig. 17. Experimental waveforms of inverter line voltage V_s and the motor terminal voltage V_m, the inverter output current I_{phase} and dc-supply current I_{dc} for the steady state experiment when the motor is supplied by (a) the two-level inverter and (b) the module-parallel inverter.



(a)



(b)

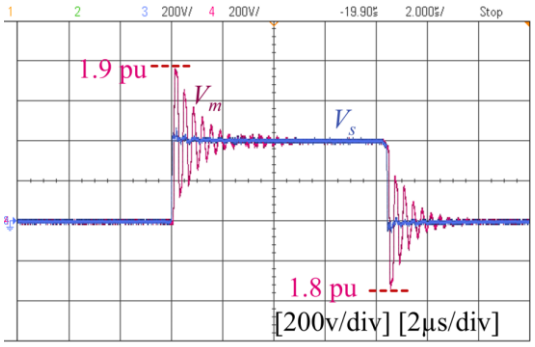
Fig. 18. Frequency domain assessment of inverter output current (a) frequency spectrum and (b) main harmonic components.

Fig. 19 shows the experimental results when the motor is supplied by the 2L inverters, where Fig. 19a shows the results for one switching cycle while Figs. 19b and 19c show the zoomed-in results, respectively. Referring to Fig. 19, the voltage at the motor terminals oscillates in a damped manner with the magnitudes of 1.9 p.u. and 1.8 p.u. at the rising and falling edges, respectively.

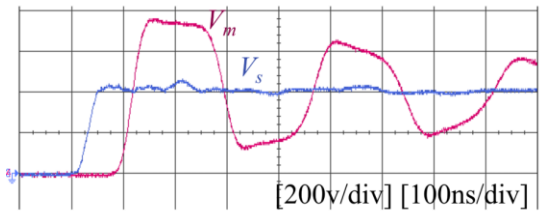
Fig. 20 shows the experimental results when the motor is supplied by the Q3L PWM-based module-parallel power inverter, where Figs. 20a-20c show inverter and motor line voltages for at the switching cycle and the rising and falling edges, respectively. Compared with the experimental results of the two-level inverter, the motor overvoltage is significantly attenuated, where the peak voltage is about 1.25 p.u., when the module-parallel inverter is employed, as shown in Fig. 20. This is because the module-parallel inverter can generate the Q3L voltage waveform at both the rising and falling edges, as shown in Figs. 20b and 20c.

Figs. 21a and 21b further show the module-parallel inverter bridge-leg output voltages V_{A1N} and V_{A2N}, and the inverter output voltage V_{AN} for the rising and falling edges, respectively. As can be noticed, while each bridge-leg generates a two-level voltage, the inverter generates a Q3L voltage, which can be used to mitigate the motor overvoltage due to the reflected wave phenomenon. In addition, the inverter output dv/dt of the module-parallel inverter is half of the output voltage of each phase-legs, as show in Fig. 21.

Figs. 22 shows the inverter bridge-leg currents I_{A1} and I_{A2}, the inverter phase current I_A, and the inverter output voltage V_A for phase A, where Figs. 22a and 22b show the results of the inverter without and with using the active current balance control approach, respectively. Referring to Fig. 22a, there is a constant offset current, which is about 2A for the two legs, when the active current balance control is not used. By contrast, the bridge-leg current can be balanced when the active current balance control approach is employed, as shown in Fig. 22b.



(a)



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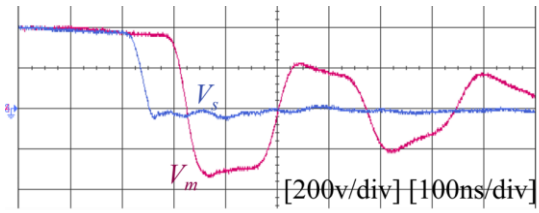


(c)

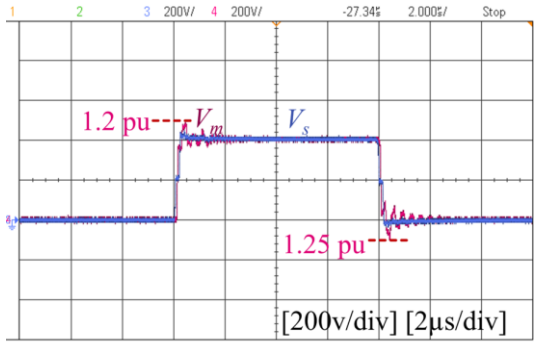
Fig. 19. Experimental waveforms of inverter line voltage V_s and the motor terminal voltage V_m when the motor is supplied by the two-level inverter for (a) one switching view, (b) extended view at the rising edge and (c) extended view at the falling edge.

Fig. 23. compares the efficiency of the two-level inverter and the Q3L module-parallel inverter at different power based on the PLECS power loss simulation. The results indicate that the two-level inverter is slightly more efficient than the Q3L module-parallel inverter, with an efficiency that is about 0.5% higher.

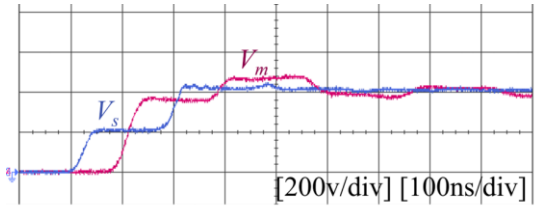
V. Conclusion

This article has proposed a Q3L PWM-based module-parallel inverter to elevate the power capacity and combat the motor overvoltage when using SiC MOSFETs in high power adjustable speed drives. The module-parallel power inverter can extend the output current capacity of the inverter because the load current can be evenly distributed among the bridge-legs. The proposed approach can generate a Q3L output voltage to mitigate the motor overvoltage. The general idea of the overvoltage mitigation mechanism has been derived in the time domain and frequency domain. The theoretical analysis shows that by actively shifting the gate signal of one bridge-leg prior to the other bridge-leg by t_{dwell}, it can mitigate the motor overvoltage significantly. The effectiveness of the Q3L PWM has been experimentally verified with the SiC bridge-leg parallel inverter-fed drives. The experimental results show that

the proposed scheme can significantly mitigate the motor overvoltage, compared with the conventional two-level inverter.



(a)



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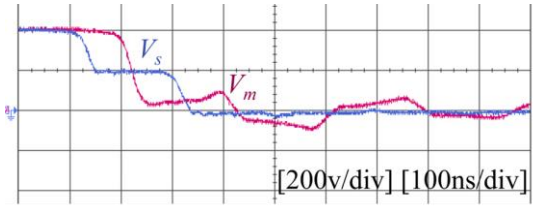
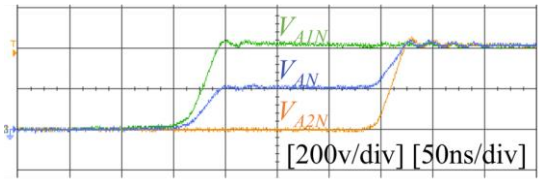
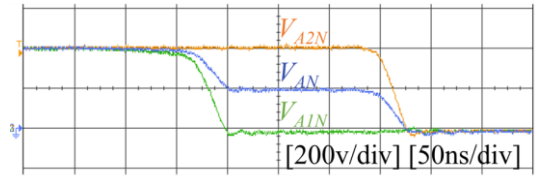


(c)

Fig. 20. Experimental waveforms of inverter line voltage V_s and the motor terminal voltage V_m when the motor is supplied by the Q3L module-parallel inverter for (a) one switching view, (b) extended view at the rising edge and (c) extended view at the falling edge.

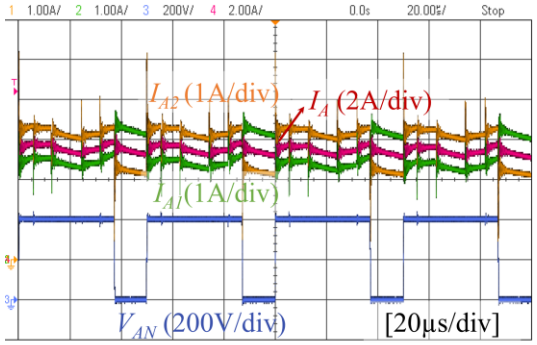


(a)

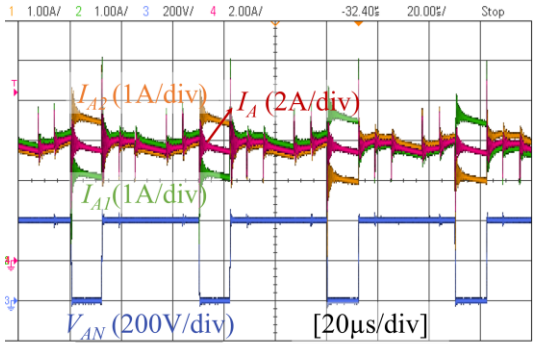


(b)

Fig. 21. Leg A1 output voltage V_{A1N}, leg A2 output voltage V_{A2N}, and phase A output voltage V_{AN} of the Q3L PWM-based module-parallel inverter.



(a)



(b)

Fig. 22. The currents of bridge-leg A1 I_{A1}, bridge-leg A1 I_{A1} bridge-leg A1 I_{A1} for the inverter (a) without and (b) with using the active current balance control approach.

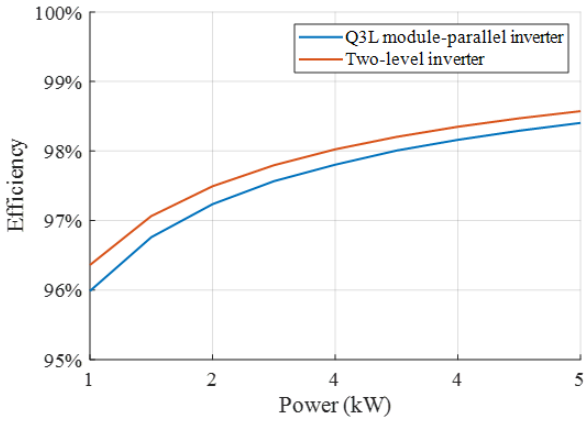


Fig. 23. Power inverter power efficiency.

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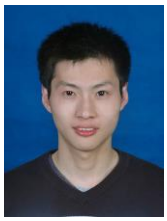

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